NOTICE OF CHANGE

INCH-POUND

The documentation and process conversion measures necessary to comply with this notice shall be completed by 5 January 2003.

MIL-STD-750D
NOTICE 5
12 November 2002

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD FOR SEMICONDUCTOR DEVICES

TO ALL HOLDERS OF MIL-STD-750D:

1. THE FOLLOWING PAGES OF MIL-STD-750D HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

NEW PAGE	DATE	SUPERSEDED PAGE	DATE
15	12 November 2002	15	30 April 2001
16	12 November 2002	16	30 April 2001
17	12 November 2002	17	30 April 2001
18	12 November 2002	18	30 April 2001
19/20	12 November 2002	19/20	30 April 2001

2. THE FOLLOWING TEST METHODS OF MIL-STD-750D HAVE BEEN REVISED AND SUPERSEDE THE TEST METHOD LISTED:

METHOD	DATE	SUPERSEDED METHOD	DATE
1018.2	12 November 2002	1018.1	30 April 2001
2071.6	12 November 2002	2071.5	30 April 2001
2074.4	12 November 2002	2074.3	23 February 1996
3131.4	12 November 2002	3131.3	30 April 2001
3306.4	12 November 2002	3306.3	28 February 1995
4023.1	12 November 2002	4023	28 February 1995

3. THE FOLLOWING NEW METHODS HAVE BEEN ADDED:

METHOD	TITLE	DATE
1057	Resistance to glass cracking	12 November 2002
3100	Junction temperature measurement	12 November 2002

4. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

5. Holders of MIL-STD-750D will verify that page changes and additions indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or canceled.

NOTE: The margins of this notice are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA – NA
DLA-CC

Review activities:
Army - AR, MI
Navy - AS, MC, SH
Air Force – 19, 99

Preparing activity:
DLA - CC

(Project 5961-2661)

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METHOD 1018.2

INTERNAL GAS ANALYSIS

1. Purpose. The purpose of this test is to measure the water-vapor content of the atmosphere inside a metal or ceramic hermetically-sealed device. It can be destructive (procedures 1 and 2) or nondestructive (procedure 3).

2. Apparatus. The apparatus for the internal water-vapor content test shall be as follows for the chosen procedure:

2.1 Procedure 1. (Procedure 1 measures the water-vapor content of the device atmosphere by mass spectrometry.) The apparatus for procedure 1 shall consist of:

a. A mass spectrometer meeting the following requirements:

(1) Spectra range. The mass spectrometer shall be capable of reading a minimum spectra range of 1 to 100 atomic mass units (AMUs).

(2) Detection limit. The mass spectrometer shall be capable of reproducibly detecting the specified moisture content for a given volume package with signal to noise ratio of 20 to 1 (i.e., for a specified limit of 5,000 parts per million volume (ppmv), .01 cc, the mass spectrometer shall demonstrate a 250 ppmv minimum detection limit to moisture for a package volume of .01 cc). The smallest volume shall be considered the worst case.

(3) Calibration. The calibration of the mass spectrometer shall be accomplished at the specified moisture limit (±20 percent) using a package simulator which has the capability of generating at least three known volumes of gas ±10 percent on a repetitive basis by means of a continuous sample volume purge of known moisture content ±10 percent. Moisture content shall be established by the standard generation techniques (i.e., 2 pressure, divided flow, or cryogenic method). The dew point analyzer shall be recalibrated a minimum of once per year using equipment traceable to NIST or by a suitable commercial calibration services laboratory using equipment traceable to NIST standards. Calibration records shall be kept on a daily basis. Gas analysis results obtained by this method shall be considered valid only in the moisture range or limit bracketed by at least two (volume or concentration) calibration points (i.e., 5,000 ppmv between .01 - .1 cc or 1,000 - 5,000 ppmv between .01 - .1 cc). A best fit curve shall be used between volume calibration points. Systems not capable of bracketing may use an equivalent procedure as approved by the qualifying activity. Corrections of sensitivity factors deviating greater than 10 percent from the mean between calibration points shall be required.

NOTE: It is recommended that the percentage of water vapor contained in a gas flowing through the gas humidifier be compared to the dewpoint sensor reading for accuracy of the sensor. The following equation may be used to calculate the percent of water vapor contained in a gas flowing through the gas humidifier.

$$\%H2O = \frac{100\ (Pv\ \text{mb})}{68.95\ \text{mb/psi}\ \ Pg + 1.33\ \text{mb/mm}\ \ Pa}$$

Where:
P_v = vapor pressure of water in the GPH based on water temperature in degrees centigrade,
P_g = gauge pressure in psi, and
P_a = atmospheric pressure in mm Hg.

*(4) Calibration for other gases. Calibration shall be required for all gases found in concentrations greater than .01 percent by volume. As a minimum, this shall include all gases listed in 3.1c. The applicable gases shall be calibrated at approximately 1 percent concentrations as part of the yearly calibration requirements, with the exception of fluorocarbons, which may use a concentration of approximately 200 ppmv; nitrogen, which may use a concentration of approximately 80 percent; helium, which may use a concentration of approximately 10 percent; and oxygen, which may use a concentration of approximately 20 percent.

(5) Calibration check. The system calibration shall be checked on the day of test prior to any testing. This shall include checking the calibration by in-letting a 5000 ppmv ±20 percent moisture calibration sample of the required volumes and comparing the result with the calibration sample. The resulting moisture reading shall be within 250 ppmv of the moisture level in the calibration sample. Calibration performed on the day of test prior to any testing may be substituted for this calibration check.

b. A vacuum opening chamber which can contain the device and a vacuum transfer passage connecting the device to the mass spectrometer of 2.1a. The system shall be maintained at a stable temperature equal to or above the device temperature. The fixturing in the vacuum opening chamber shall position the specimen as required by the piercing arrangement of 2.1c, and maintain the device at 100°C ±5°C for a minimum of 10 minutes prior to piercing.

NOTE: A maximum 5 minute transfer time from prebake to hot insertion into apparatus shall be allowed. If 5 minutes is exceeded, device shall be returned to the prebake oven and prebake continued until device reaches 100°C ± 5°C.

For initial certification of systems or extension of suitability, device temperature on systems using an external fixture shall be characterized by placing a thermocouple into the cavity of a blank device of similar mass, internal volume, construction and size. This shall be a means for proving the device temperature has been maintained at 100°C ± 5°C for the minimum 10 minutes. This also applies to devices prebaked in an external oven but tested with the external fixture to adjust for any temperature drop during the transfer. These records shall be maintained by the test laboratory.

c. A piercing arrangement functioning within the opening chamber or transfer passage of 2.1b, which can pierce the specimen housing (without breaking the mass spectrometer chamber vacuum and without disturbing the package sealing medium), thus allowing the specimen's internal gases to escape into the chamber and mass spectrometer.

NOTE: A sharp-pointed piercing tool, actuated from outside the chamber wall via a bellows to permit movement, should be used to pierce both metal and ceramic packages. For ceramic packages, the package lid or cover should be locally thinned by abrasion to facilitate localized piercing.

2.2 Procedure 2. (Procedure 2 measures the water-vapor content of the device atmosphere by integrating moisture picked up by a dry carrier gas at 50°C.) The apparatus for procedure 2 shall consist of:

a. An integrating electronic detector and moisture sensor capable of reproducibly detecting a water-vapor content of 300 ppmv ±50 ppmv moisture for the package volume being tested. This shall be determined by dividing the absolute sensitivity in micrograms H_20 by the computed weight of the gas in the device under test, and then correcting to ppmv.

b. A piercing chamber or enclosure, connected to the integrating detector of 2.2a, which will contain the device specimen and maintain its temperature at 100°C ±5°C during measurements. The chamber shall position the specimen as required by the piercing arrangement. The piercing mechanism shall open the package in a manner which will allow the contained gas to be purged out by the carrier gas or removed by evacuation. The sensor and connection to the piercing chamber will be maintained at a temperature of 50°C ±2°C.

2.3 Procedure 3. (Procedure 3 measures the water-vapor content of the device atmosphere by measuring the response of a calibrated moisture sensor or an IC chip which is sealed within the device housing, with its electrical terminals available at the package exterior.) The apparatus for procedure 3 shall consist of one of the following:

a. A moisture sensor element and readout instrument capable of detecting a water-vapor content of 300 ppmv ±50 ppmv while sensor is mounted inside a sealed device.

b. Metallization runs on the device being tested isolated by back-biased diodes which when connected as part of a bridge network can detect 2,000 ppmv within the cavity. The chip shall be cooled in a manner such that the chip surface is the coolest surface in the cavity. The device shall be cooled below dew point and then heated to room temperature as one complete test cycle.

NOTE: Suitable types of sensors may include (among others) parallel or interdigitated metal stripes on an oxidized silicon chip, and porous anodized-aluminum structures with gold-surface electrodes.

Surface conductivity sensors may not be used in metal packages without external package wall insulation. When used, the sensor shall be the coolest surface in the cavity. It should be noted that some surface conductivity sensors require a higher ionic content than available in ultraclean CERDIP packages. In any case, correlation with mass spectrometer procedure 1 shall be established by clearly showing that the sensor reading can determine whether the cavity atmosphere has more or less than the specified moisture limit at 100°C.

3. Procedure. The internal water-vapor content test shall be conducted in accordance with the requirement of procedure 1, procedure 2, or procedure 3. All devices shall be prebaked for 16 to 24 hours at 100°C ±5°C prior to hot insertion into apparatus. External ovens shall have a means to indicate if a power interuption occurs during the prebaking period and for how long the temperature drops below 100°C ± 5°C. Devices baked in an external oven which loses power and whose temperature drops below 100°C ± 5°C for more than 1 hour shall undergo another prebake to begin a minimum of 12 hours later.

NOTE: It is recommended that samples submitted to the labs shall include information about the manufacturing process including sealing temperature, sealing pressure, sealing gas, free internal cavity volume, lid thickness at puncture site, lid material, and the location of the puncture site.

3.1 Procedure 1. The device shall be hermetic in accordance with test method 1071, and free from any surface contaminants which may interfere with accurate water-vapor content measurement.

After device insertion, the device and chamber shall be pumped down and baked out at a temperature of 100°C ±5°C until the background pressure level will not prevent achieving the specified measurement accuracy and sensitivity. After pumpdown, the device case or lid shall be punctured and the following properties of the released gases shall be measured, using the mass spectrometer:

a. The increase in chamber pressure as the gases are released by piercing the device package. A pressure rise of less than 50 percent of normal for that package volume and pressurization may indicate that (1) the puncture was not fully accomplished, (2) the device package was not sealed hermetically, or (3) does not contain the normal internal pressure.

b. The water-vapor content of the released gases, as a percent by unit volume or ppmv of the total gas content.

c. The proportions (by volume) of the other following gases: N_2, He, Mass 69 (fluorocarbons), O_2, Ar, H_2, CO_2, CH_4, NH_3, and other solvents, if available. Calculations shall be made and reported on all gases present greater than .01 percent by volume. Data reduction shall be performed in a manner which will preclude the cracking pattern interference from other gas specie in the calculations of moisture content. Data shall be corrected for any system dependent matrix effects such as the presence of hydrogen in the internal ambient.

3.1.1 Failure criteria.

a. A device which has a water-vapor content greater than the specified maximum value shall constitute a failure.

b. A device which exhibits an abnormally low total gas content, as defined in 3.1a, shall constitute a failure, if it is not replaced. Such a device may be replaced by another device from the same population; if the replacement device exhibits normal total gas content for its type, neither it nor the original device shall constitute a failure for this cause.

3.2 Procedure 2. The device shall be hermetic in accordance with test method 1071, and free from any surface contaminants which may interfere with accurate water-vapor content measurement.

After device insertion into the piercing chamber, gas shall be flowed through the system until a stable base-line value of the detector output is attained. With the gas flow continuing, the device package shall then be pierced so that a portion of the purge gas flows through the package under test and the evolved moisture integrated until the base-line detector reading is again reached. An alternative allows the package gas to be transferred to a holding chamber which contains a moisture sensor and a pressure indicator. System is calibrated by injecting a known quantity of moisture or opening a package of known moisture content.

3.2.1 Failure criteria.

a. A device which has a water-vapor content (by volume) greater than the specified maximum value shall constitute a failure.

b. After removal from the piercing chamber, the device shall be inspected to ascertain that the package has been fully opened. A device package which was not pierced shall constitute a failure, if the test is not performed on another device from the same population; if this retest sample or replacement is demonstrated to be pierced and meets the specified water-vapor content criteria, the specimen shall be considered to have passed the test.

c. A package which is a leaker in the purge case will be wet and counted as a failure. In the case of evacuation, a normal pressure rise shall be measured as in 3.1a.

3.3 Procedure 3. The moisture sensor shall be calibrated in an atmosphere of known water-vapor content, such as that established by a saturated solution of an appropriate salt or dilution flow stream. It shall be demonstrated that the sensor calibration can be verified after package seal or that post seal calibration of the sensor by lid removal is an acceptable procedure.

The moisture sensor shall be sealed in the device package or, when specified, in a dummy package of the same type. This sealing shall be done under the same processes, with the same die attach materials and in the same facilities during the same time period as the device population being tested.

The water-vapor content measurement shall be made, at 100°C or below, by measuring the moisture sensor response. Correlation with procedure 1 shall be accomplished before suitability of the sensor for procedure 3 is granted. It shall be shown the package ambient and sensor surface are free from any contaminating materials such as organic solvents which might result in a lower than usual moisture reading.

3.3.1 Failure criteria. A specimen which has a water-vapor content greater than the specified maximum value shall constitute a failure.

4. Implementation. Suitability for performing method 1018 analysis is granted by the qualifying activity for specific limits and volumes. Method 1018 calibration procedures and the suitability survey are designed to guarantee ±20 percent lab-to-lab correlation in making a determination whether the sample passes or fails the specified limit. Water vapor contents reported either above or below (water vapor content - volume) the range of suitability are not certified as correlatable values. This out of specification data has meaning only in a relative sense and only when one laboratory's results are being compared. The specification limit of 5,000 ppmv shall apply to all package volumes, with the following correction factors permitted, to be used provided they are documented and shown to be applicable:

For package volumes less than .01 cc internal free volume which are sealed while heated in a furnace:

$$C_T = \frac{T_r + 273}{T_s + 273}$$

Where:
C_T = correction factor (temperature)
T_r = room temperature (°C)
T_s = sealing temperature (°C).

For package volumes of any size sealed under vacuum conditions:

$$C_P = \frac{P_s}{P_a}$$

C_P = correction factor (pressure)
P_s = sealing pressure
P_a = atmospheric pressure (pressures may be in Torr or mm Hg).

The correction factor, if used, shall be applied as follows:

Water vapor (corrected) = Water vapor (measured) x C_X; where C_X is the applicable correction factor.

The range of suitability for each laboratory will be extended by the qualifying activity when the analytical laboratories demonstrate an expanded capability. Information on current analytical laboratory suitability status can be obtained by contacting Defense Supply Center, Columbus, ATTN: DSCC-VQE, P.O. Box 3990, Columbus, OH 43216-5000.

5. Summary. The following details shall be specified in the applicable acquisition document:

a. The procedure (1, 2, or 3) when a specific procedure is to be used (see 3).

b. The maximum allowable water-vapor content falling within the range of suitability as specified MIL-PRF-19500.

* 6. Surrogate monitors. Surrogate monitors are only applicable for packages less than .01 cc to evaluate the process baseline. Surrogate monitors will be subject to RGA testing in accordance with method 1018 herein. A production lot will be validated by the performance of its monitors. It is well known and established that preseal bake and storage conditions of packaging materials will severely impact the levels of moisture detected in almost any package type. The use of the surrogate monitors without a controlled and disciplined manufacturing line is of questionable value. The proposed test is not, nor is it intended to be a direct measurement of small packaged product internal moisture. However, it is a quantifiable indicator that the process and controls used are consistent. This is an improvement over the existing situation in which there is a requirement for control of internal moisture and no accurate and repeatable method of measurement.

* 6.1. Requirements. Surrogate monitors are to be procured from the same manufacturer and be manufactured in the same technology as the production headers, using the same materials, plating, processing and technology. For example, the UB packages: Kyocera header, multilayer cofired ceramic technology; SemiAlloys lid, Alloy 52, nickel underplate, gold plate.

a. The device manufacturer shall use the same preconditioning on surrogate monitors and production product, i.e. vacuum bake time and temperature, storage conditions, die attach materials and process, etc.

b. Surrogate monitors shall be sealed at the same time and using the same process as the production parts.

c. To optimize the effect of preconditioning the transit time from the oven to the seal furnace shall be controlled and minimal.

d. A typical process would include:

(1) Batch high-vacuum bake headers and lids.

(2) Store baked material in dry nitrogen.

(3) Second vacuum bake overnight (min. 12 hrs) just prior to seal.

(4) Minimize the post-2nd bake exposure to atmosphere.

e. Surrogate monitor packages will be under baseline documentation control. Full traceability from procurement to utilization shall be maintained.

f. Initially, the surrogate monitors will be used at the beginning of the seal operation and at 2 hour intervals. A minimum of six monitors must be processed for each seal lot (a "seal lot" may consist of multiple production lots if they go through sealing without interruptions (other than the scheduled breaks) and have identical traceability of headers and lids).

g. It is expected that it will take approximately 6 months for a manufacturer to collect enough lots and data to establish a baseline. Later modifications of the preconditioning process will be evaluated against this baseline.

h. The device manufacturer will submit to DSCC the results from a minimum of three "seal" lots to establish the effectiveness of the process baseline. Additional testing will be retained and available to DSCC upon request.

METHOD 1057

RESISTANCE TO GLASS CRACKING

1. Purpose. This method provides a means of judging the relative resistance of glass encapsulated electronic components to cracking under conditions of thermal stress. It employs immersion in a hot liquid then water to simulate the thermal stresses associated with both device manufacturing processes and end user assembly procedures.

2. Apparatus. Liquid baths shall be used which are capable of providing and maintaining the specified temperatures in the working zone when loaded with a maximum load. Bath temperatures under maximum load conditions shall be verified as needed to validate bath performance. Liquid composition shall be as specified herein.

3. Procedure. Remove any paint or other surface coatings. Clean test specimens using a general purpose cleaner/degreaser and rinse in water then acetone. Subsequent to cleaning, specimens shall be placed into the baths defined in table I for the applicable test condition using a dipping tool that will not significantly heat sink the body of the device under test. Specimens shall be fully immersed in the first bath for the specified period of time then transferred immediately to and fully immersed in the second bath. Unless otherwise specified, the test shall be considered complete upon removal of the specimen from the second bath.

3.1 Timing. Specimens shall be immersed into and removed from the first (hot) bath at a rate of 1.0 ±0.5 inch (25.4 ±12.7 mm) per second. The maximum dwell time above the hot bath prior to immersion shall be 7.0 seconds. Dwell time in the hot bath shall be 6 ±1.0 seconds. Specimens shall be released completely into the second bath within 3 seconds of their removal from the hot bath.

4. Failure criteria. Specimens that fail to meet the glass crack criteria of method 2074 of MIL-STD 750 shall be considered rejects.

5. Summary. The following shall be specified in the applicable performance specification.

a. Sample size and acceptance number.

b. Test condition.

c. Special fixturing as applicable.

d. Number of test cycles if other than 1 cycle.

TABLE I. Conditions and temperatures.

Step		Test condition and temperatures	
		A	B
1	Temperature and tolerance	100°C ±5°C	235°C ±5°C
	Recommended fluid	Water	Molten solder
2	Temperature and tolerance	0°C ±5°C	25°C ± 5°C
	Recommended fluid	Water	Water

METHOD 2071.6

VISUAL AND MECHANICAL

1. Purpose. The purpose of this test is to verify the workmanship of hermetically packaged devices. This method shall also be utilized to inspect for damage due to handling, assembly, and test of the packaged device. This test is normally employed at outgoing inspection within the device manufacturer's facility, or as an incoming inspection of the assembled device.

2. Apparatus. Apparatus used in this test shall be capable of demonstrating device conformance to the applicable requirements of the individual specification. This includes optical equipment capable of magnification of 3X minimum to as specified herein, with a large field of view such as an illuminated ring magnifier.

3. Procedure. Unless otherwise specified, the device shall be examined under a magnification of 3X minimum. The field of view shall be sufficiently large to contain the entire device and allow inspection to the criteria listed in 3.1. Where inspection at a lower magnification reveals an anomaly, then inspection at a higher magnification (10X maximum, unless otherwise specified) may be performed to determine acceptability.

When a disposition is in doubt for any dimensional criteria, that dimension may be measured for verification.

3.1 Failure criteria. Devices which exhibit any of the following shall be considered rejects.

3.1.1 Rejects. Device construction (package outline), lead (terminal), identification, markings (content, placement, and legibility), and workmanship not in accordance with the applicable specification shall be rejected. This includes the following:

a. Any misalignment of component parts to the extent that the package outline drawing dimensions are exceeded.

b. Visual evidence of corrosion or contamination. Discoloration is not sufficient cause for rejection. The presence of lead carbonate formations in the form of a white/yellow crystalline shall be considered evidence of contamination.

c. Damaged or bent leads or terminals which precludes their use in the intended application.

d. Defective finish: Evidence of blistering, or evidence of nonadhesion, peeling, or flaking which exposes underplate or base metal.

e. Burrs that will cause lead or terminal dimensions to be exceeded.

f. Foreign material (including solder or other metallization) bridging leads or otherwise interfering with the normal application of the device. Where adherence of foreign material is in question, devices may be subjected to a clean filtered air stream (suction or expulsion) or an isopropyl alcohol wash and then reinspected.

g. Protrusions beyond seating plane that will interfere with proper seating of the device.

h. Missing welds or crimps.

i. Damage causing distortion of a flange beyond its normal configuration.

j. Damage to a stud (thread damage or bending) which restricts normal mounting.

k. Dents in metal lids which precludes their use in the intended application or causing a defect in the finish (see 3.1.1.d).

l. Gaps, separations, or other openings that are not part of the normal design configuration.

m. Tubulation weld: Any fracture or split in the tubulation weld.

n. Weld alignment: Base weld mating surfaces not parallel, or that precludes intended use.

3.1.1.1 Failure criteria for lead/terminal seal area of metal can devices.

a. Radial cracks (except meniscus cracks) that extend more than one-half of the distance from the pin to the outer member (see figure 2071-1). Radial cracks that originate from the outer member.

b. Circumferential cracks (except meniscus cracks) that extend more than 90 degrees around the seal center (see figure 2071-2).

c. Open surface bubble(s) in strings or clusters that exceed two-thirds of the distance between the lead and the package wall.

d. Visible subsurface bubbles that exceed the following:

(1) Large bubbles or voids that exceed one-third of the glass sealing area (see figure 2071-3).

(2) Single bubble or void that is larger than two-thirds of the distance between the lead and the package wall at the site of the inclusion and extends more than one-third of the glass seal depth (see figure 2071-4).

(3) Two bubbles in a line totaling more than two-thirds of the distance from pin to case (see figure 2071-5).

(4) Interconnecting bubbles greater than two-thirds of the distance between pin and case (see figure 2071-6).

e. Except as designed, reentrant seals which exhibit non-uniform wicking or negative wicking.

f. Twenty-five percent or greater of the radius length from the center of the feedthrough to the edge of the glass eyelet.

g. Glass meniscus cracks that are not located within one-half of the distance between the lead to the case (see figure 2071-7). The glass meniscus is defined as that area of glass that wicks up the lead or terminal.

h. Any chip-out of ceramic or sealing glass that penetrates the sealing glass deeper than the glass meniscus plane. Exposed base metal as a result of meniscus chip outs are acceptable if the exposed area is no deeper than 0.010 inch (0.25 mm) or 50 percent of lead diameter, whichever is greater (see figure 2071-8).

3.1.1.2 Failure criteria for ceramic packages. Failure criteria for ceramic packages (see method 2009 of MIL-STD-883).

3.1.1.3 Failure criteria for opaque glass body devices. Failure criteria for opaque glass body devices (see method 2068 of MIL-STD-750).

* 3.1.1.4 Transparent glass diodes, double plug construction.

a. Any evidence of a crack, fracture, or a chipout closer to the die than 50 percent of the designed seal length shall be rejected. Area of examination shall be as shown on figure 2071-9.

b. Any crack that terminates in the axial direction is cause for rejection

c. Meniscus cracks are not cause for rejection.

d. Any chip out that exposes base metal shall be rejected.

* 3.1.1.5 Transparent glass diodes, large cavity (i.e. S-bend, C-bend, or straight-through constructions). Any crack or fracture in the glass over the area of the device cavity shall be rejected.

a. Any crack or fracture in the glass over the area of the device cavity shall be rejected.

b. Any chip out that exposes base metal shall be rejected (this does not apply to chipouts at either end of device where glass joins external lead).

c. Any crack that terminates in the axial direction is cause for rejection.

d. Meniscus cracks are not cause for rejection.

3.1.1.6 Failure criteria for hermetic packages with ceramic eyelet feedthroughs.

a. Any separation or delamination of the braze metallization from the inner diameter (ID) or outer diameter (OD) of the ceramic eyelet (see figures 2071-10 and 2071-11).

b. Any cracks or separation in the braze between the ceramic eyelet ID and the lead or the ceramic eyelet OD and the package. Any voids, depressions, or pinholes the bottom of which cannot be seen at 30X maximum magnification in the braze between the ceramic eyelet ID and the lead or the ceramic eyelet OD and the package.

c. Any discontinuation in the braze from the ceramic eyelet ID to the lead or the ceramic eyelet OD to the package exposing unplated metallization or bare ceramic.

d. Any conductive material attached to the ceramic eyelet that reduces the designed isolation width by more than one-third unless it is demonstrated that the device voltage isolation requirement can be met with less than two-thirds of the width of the ceramic eyelet (see figures 2071-16 through -26).

e. Any metallization that extends beyond the height of the ceramic that is not adhered to the ceramic.

f. No cracks are allowed. Chipouts greater than .005 inches (0.127 mm) in any direction are not allowed.

4. Summary. The following details shall be specified in the applicable acquisition document:

a. Requirements for markings and the lead (terminal) or pin identification.

b. Detailed requirements for materials, design, construction, and workmanship.

c. Magnification requirements, if other than specified.

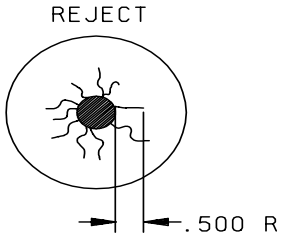


FIGURE 2071-1. Radial cracks extending more than one-half the distance from pin to outer member.

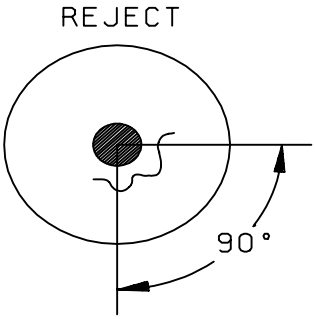


FIGURE 2071-2. Circumferential cracks.

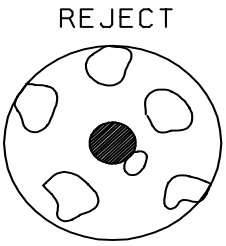


FIGURE 2071-3. Bubbles in glass exceeding one-third of the sealing area.

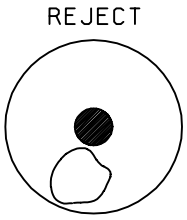


FIGURE 2071-4. Single bubble or void.

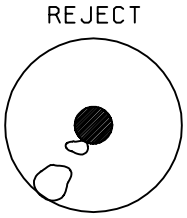


FIGURE 2071-5. Two bubbles in a line.

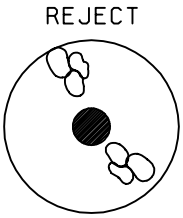


FIGURE 2071-6. Interconnecting bubbles.

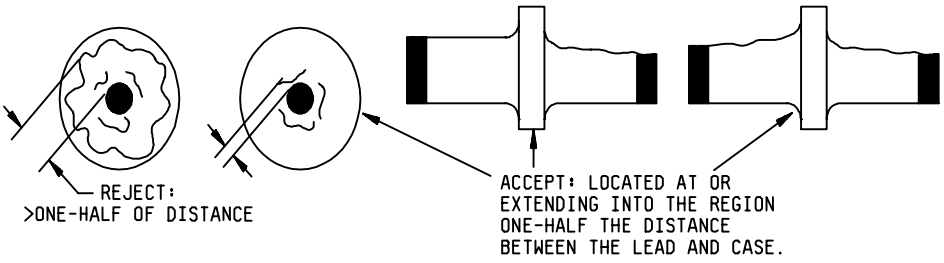


FIGURE 2071-7. Meniscus cracks.

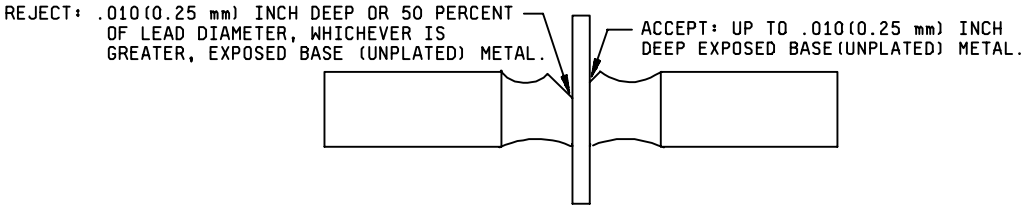


FIGURE 2071-8. Chip outs.

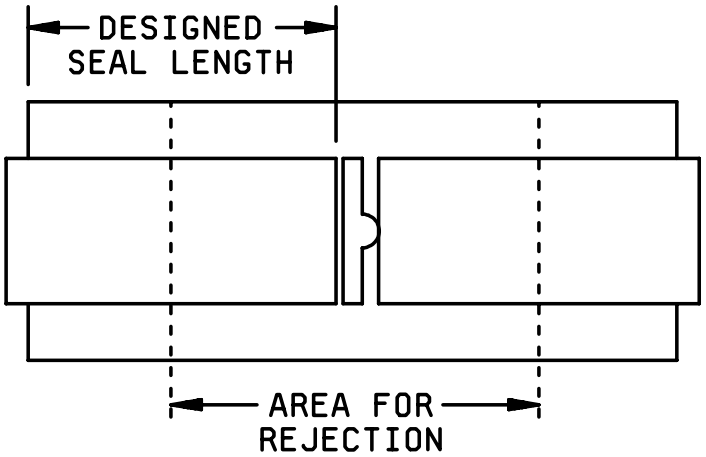
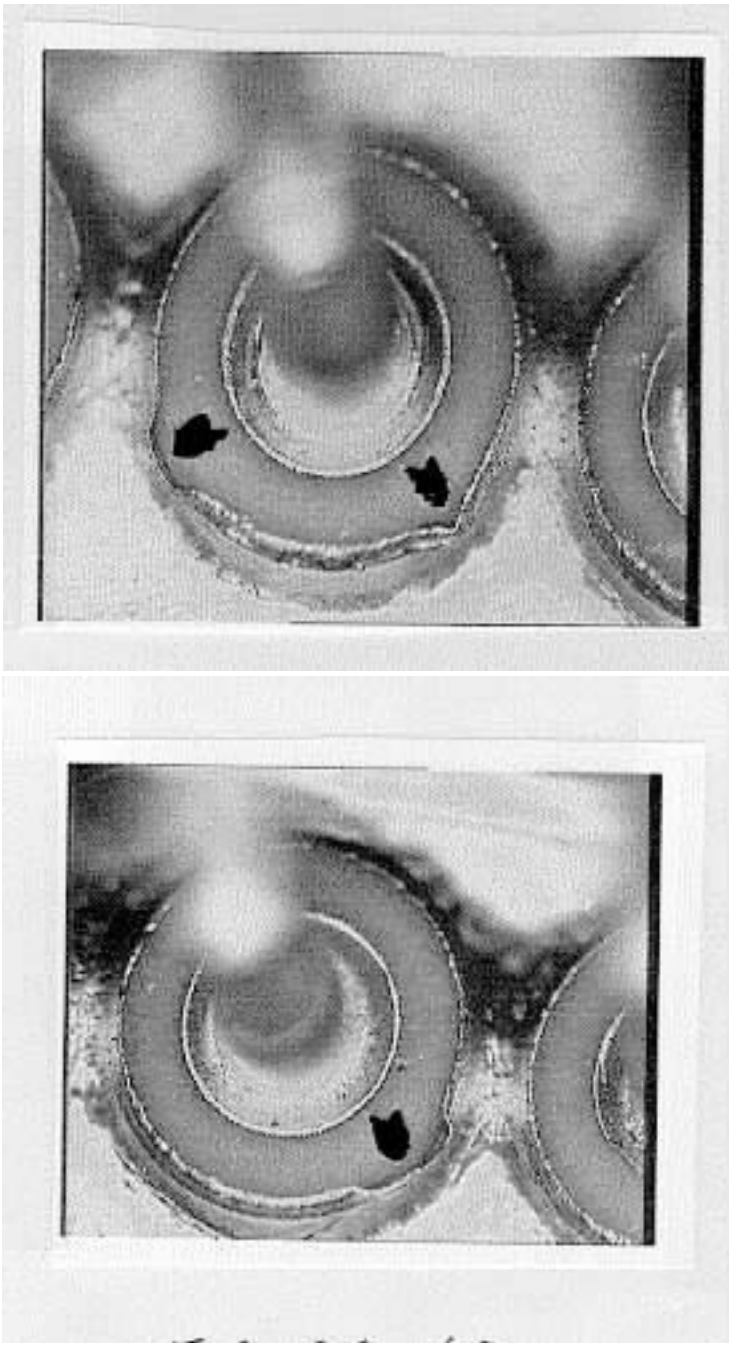
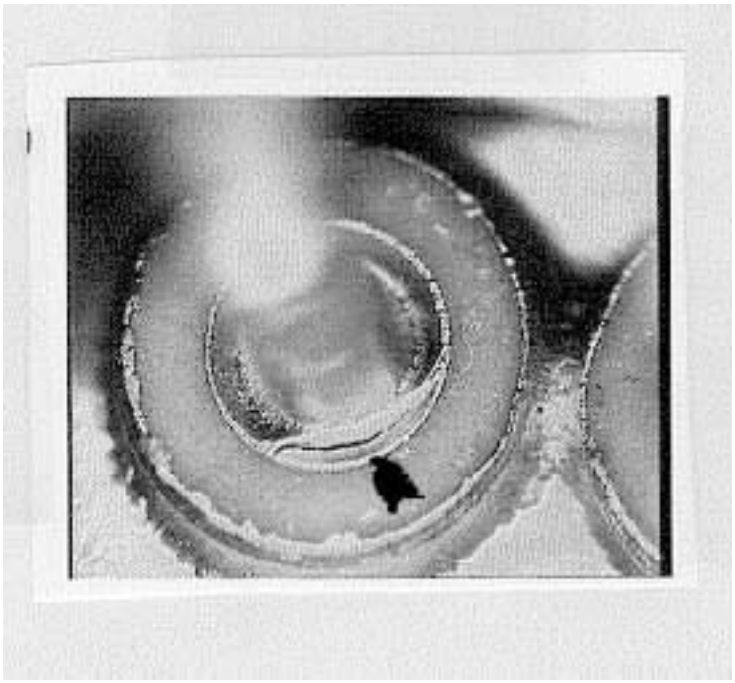


FIGURE 2071-9. Transparent glass diode (double plug construction).



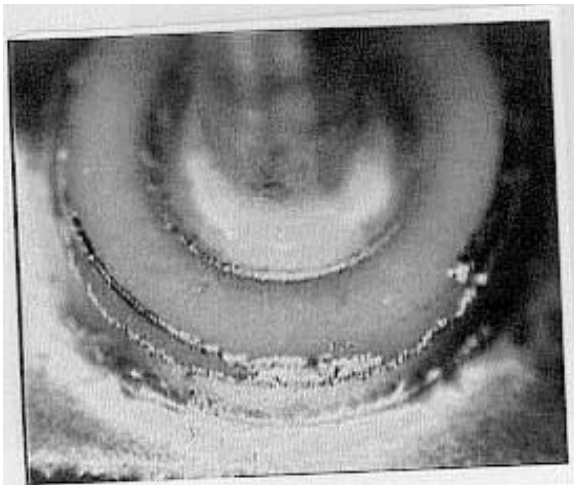
Arrows on both pictures illustrate rejectable conditions of braze separation/delamination.

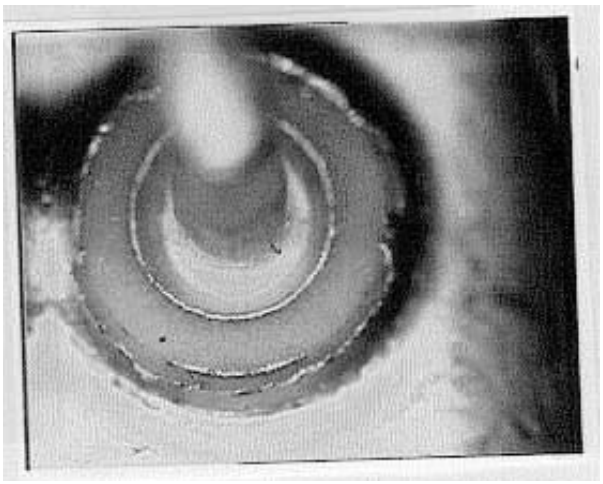
FIGURE 2071-10. Braze separation/delamination.

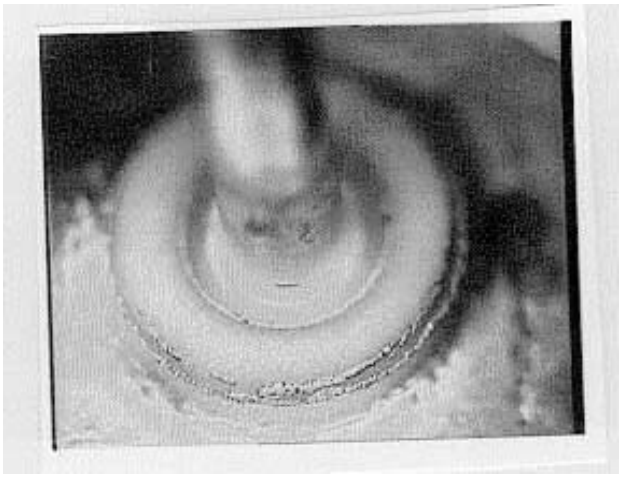


Reject: Arrow indicates a crack on the inner diameter braze metallization of the ceramic eyelet.

FIGURE 2071-11. Crack (braze metallization.







Reject: All three figures illustrate discontinuous braze metallization on the outer diameter of the ceramic eyelet.

FIGURE 2071-12. Discontinuous braze metallization.

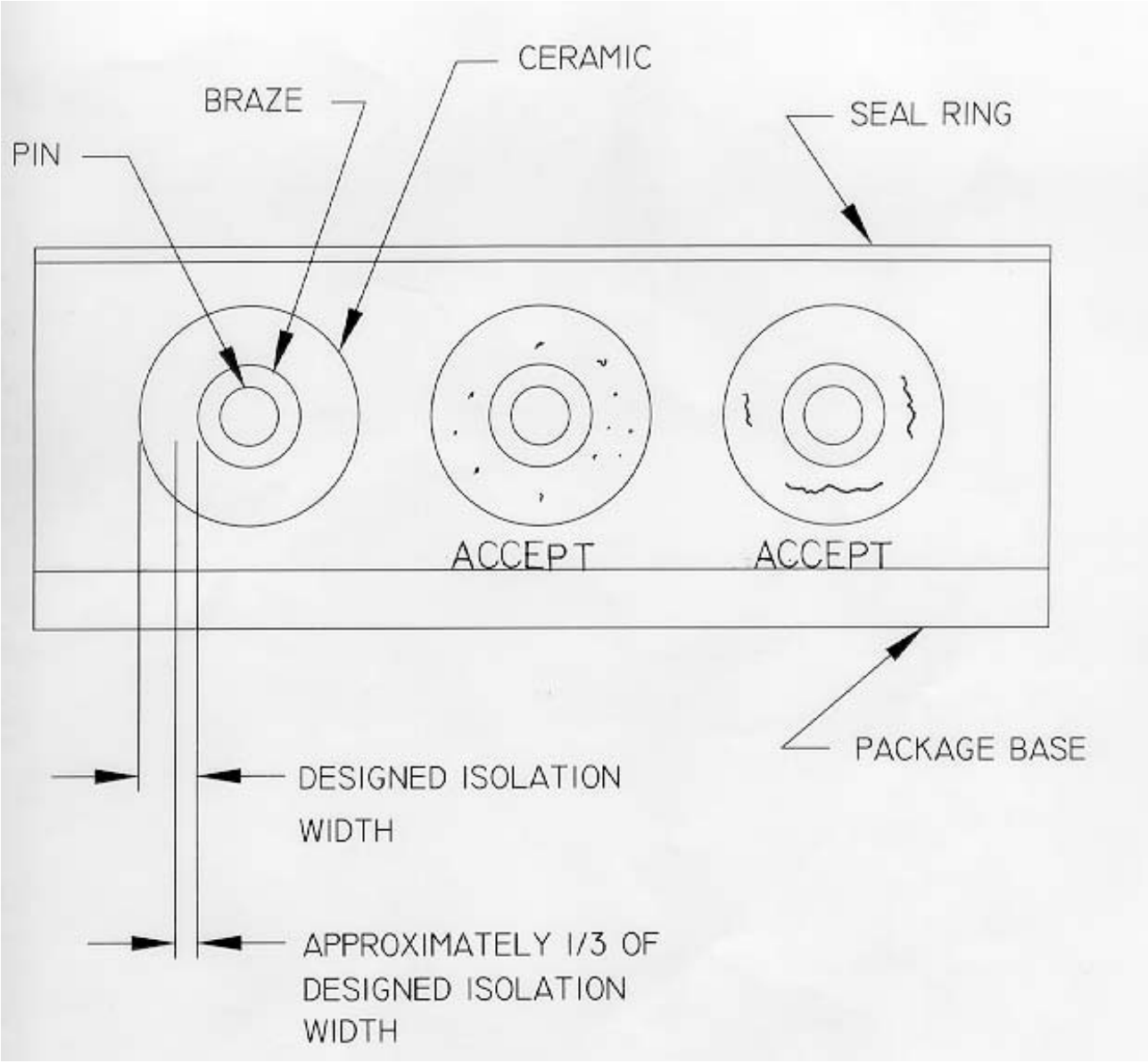
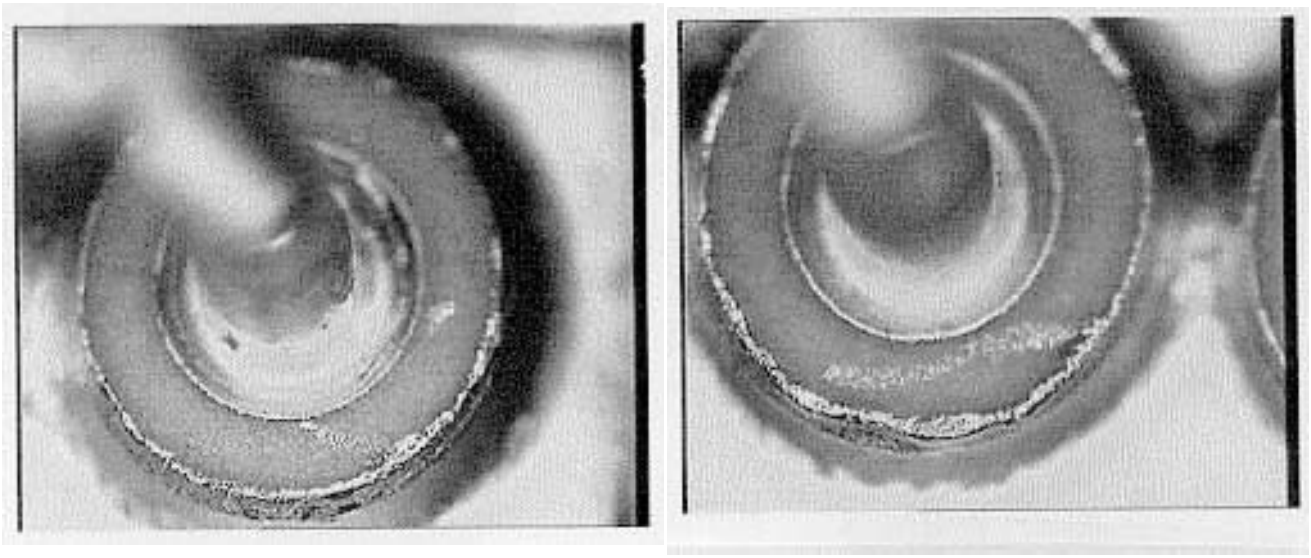
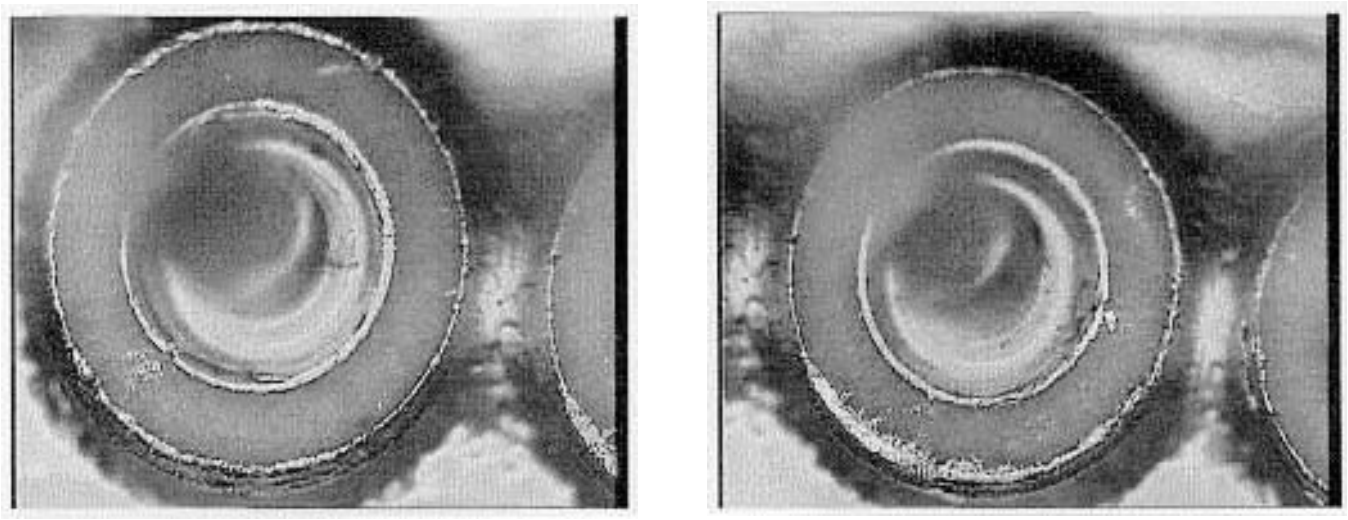


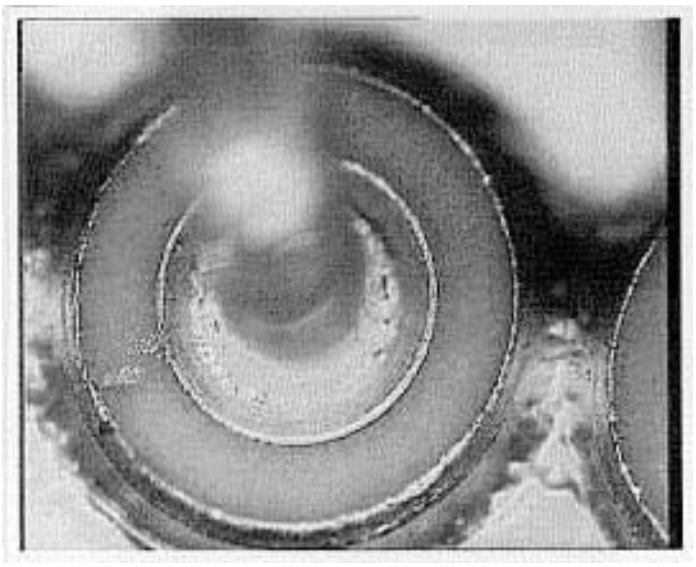
FIGURE 2071-13. Ceramic feedthrough visual inspection criteria.

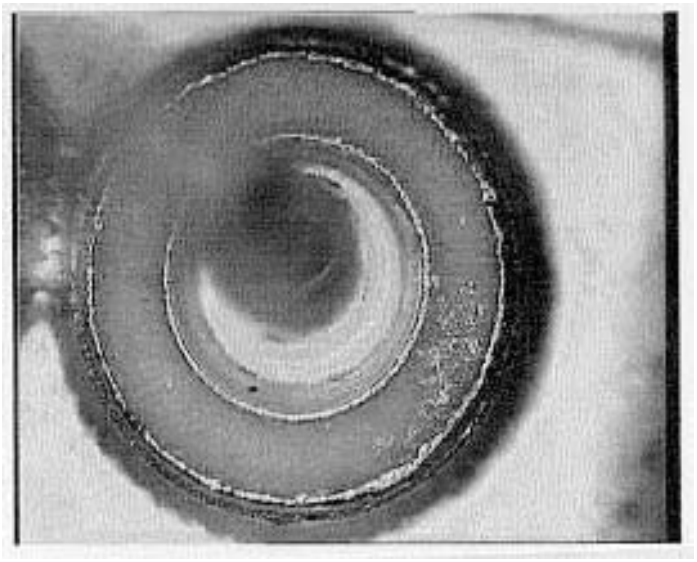


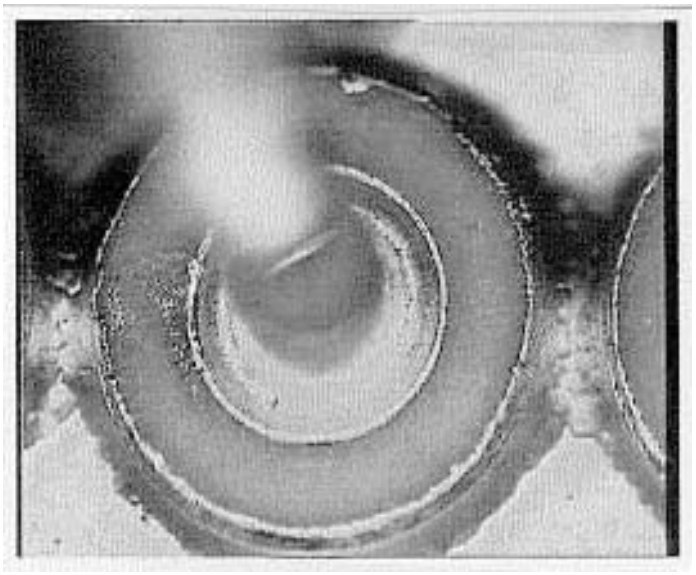


Reject: All figures indicate rejectable foreign material conditions.

FIGURE 2071-14. Rejectable foreign material conditions.

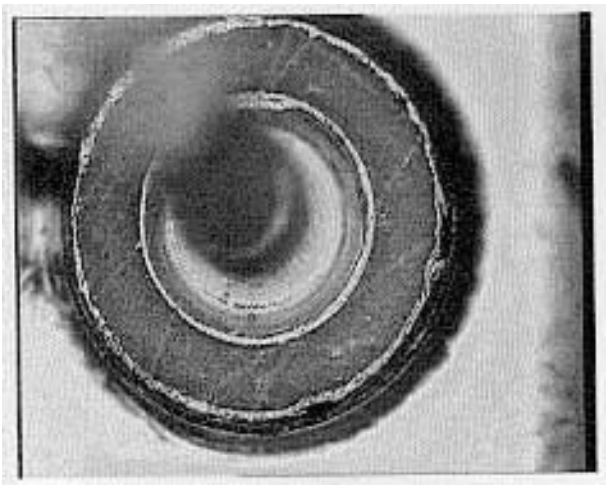


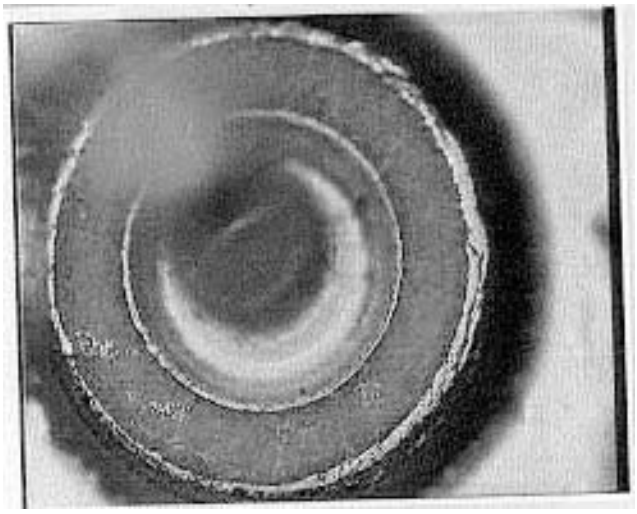


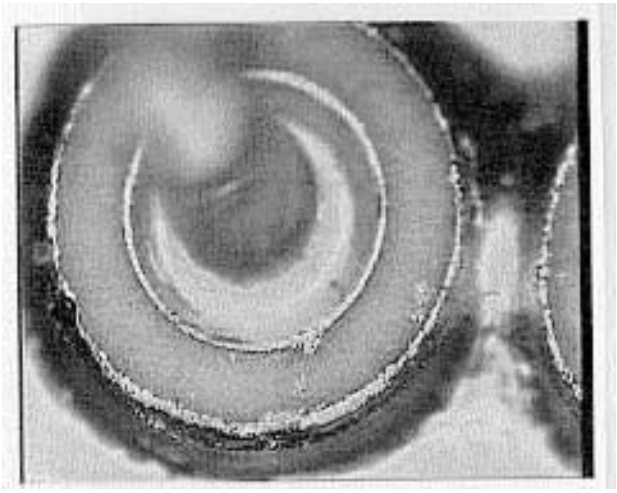


Reject: All figures indicate rejectable foreign material conditions.

FIGURE 2071-14. Rejectable foreign material conditions .







Reject: All figures indicate rejectable foreign material conditions.

FIGURE 2071-14. Rejectable foreign material conditions.

METHOD 2074.4

INTERNAL VISUAL INSPECTION (DISCRETE SEMICONDUCTOR DIODES)

1. Purpose. The purpose of this test is to check the materials, design, construction, and workmanship of discrete semiconductor diodes and other two-terminal semiconductor devices described herein. All tests shall be performed to detect and eliminate those devices with defects that could lead to device failures. Opaque glass type constructions shall be examined before encapsulation. (After encapsulation, see method 2068 of MIL-STD-750). Metal can devices shall be examined before capping. (After capping or sealing, see method 2071 of MIL-STD-750). Clear glass construction shall be examined after encapsulation.

2. Apparatus.

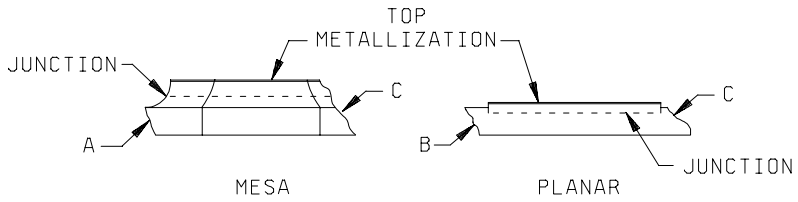
a. The apparatus for these tests shall include optical equipment and any visual standards (e.g., gauges, drawings, photographs) necessary to perform an effective examination and enable the operator to make objective decisions on the acceptability of the device being examined. Any necessary fixturing for handling devices during examination to promote efficient operation without damaging the units shall be provided.

b. A monocular, binocular, or stereo microscope capable of magnification from 20X minimum to 30X maximum, shall be used unless otherwise specified. The inspection shall be performed under suitable illumination.

* 3. Procedure. The devices shall be examined at the specified magnifications to determine compliance with the requirements of the applicable sections of this test method based on device construction. Examinations for transparent body devices may be performed anytime prior to body coating or painting. Axial construction devices shall be viewed at approximate right angles to their major axis while being rotated through 360 degrees. For the time interval, if any, between visual inspection and package sealing, devices shall be stored, handled, and processed in a manner to avoid contamination and to preserve the integrity of the devices as inspected.

* 3.1 Die criteria (applicable to all body styles).

a. Chipouts. Reject for chipouts that extend more than 50 percent of the way up the moat area (mesa devices) or that extend to within 2 mils of the junction. NOTE: Actual junction location will vary depending on specific device characteristics. (Figure 2074-1.)

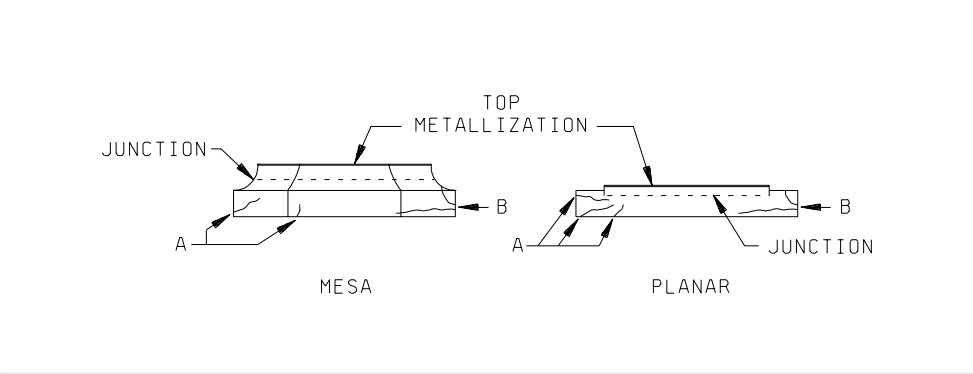


ACCEPT: CHIPOUTS ≤ 50% UP MOAT AND ≥ 2 MILS FROM JUNCTION - "A"
ACCEPT: CHIPOUTS ≥ 2 MILS FROM JUNCTION - "B"
REJECT: CHIPOUTS ≤ 2 MILS FROM JUNCTION - "C"

* FIGURE 2074-1. Chipouts.

* b. Cracks. Reject for cracks that extend to within 2 mils of the junction or propagate in the direction of the junction. NOTE: The junction may be in a different place than shown depending on specific device characteristics.

REJECT: CRACKS ≤ 2 MILS FROM JUNCTION OR PROPAGATING TOWARD JUNCTION -"A"
ACCEPT: CRACKS ≥ 2 MILS FROM JUNCTION AND PROPAGATING AWAY FROM JUNCTION -"B"



* FIGURE 2074-2. Cracks.

* 3.2 Applicable body styles. The devices shall be examined in accordance with the following addendums as applicable for the body style involved.

Addendum A Axial lead, transparent body, pressure contact design

Addendum B Axial lead, transparent body straight through lead to die contact

Addendum C Axial lead and surface mount, double plug transparent body (dumet plug, round end cap, soft glass)

Addendum D Axial lead and surface mount, double plug transparent body (tungsten or molybdenum plug, square end cap, hard glass)

Addendum E Axial lead, transparent body, point contact

Addendum F Axial lead, double plug, opaque body, power rectifier and regulator

Addendum G Metal body, axial lead, solder contact design

Addendum H Metal body, stud mounted, solder contact design

Addendum I Metal body, diamond base regulators, solder contact design

4. Summary.

a. Detailed requirements for materials, design, construction, and workmanship.

b. Magnification requirements, if other than specified.

APPENDIX A

SMALL SIGNAL, COMPUTER, REGULATOR, LOW POWER RECTIFIERS, AND MICROWAVE DIODES

A.1 Axial lead, transparent body, pressure contact design. The following examinations shall be made after encapsulation (C and S bend whisker).

A.1.1 Glass cracks and chips (see figure 2074-A1). No cracks shall be allowed in the vicinity of the cavity. Any crack originating at either end of the package or crack that extends into the body of the glass toward the cavity more than 25 percent of the glass-to-glass or glass-to-metal seal length shall be cause for rejection. Any glass chip deep enough to expose the plug or lead surface and extending longitudinally into the glass-to-metal seal toward the cavity to reduce the effective seal length to less than one external lead diameter shall be cause for rejection.

A.1.2 Incomplete seal. All devices shall be inspected for glass-to-metal seal or glass-to-glass seal. Both seals shall be a minimum of one external lead diameter over the entire sealed portion (sealed interface).

A.1.3 Bubbles in seal. All devices shall be inspected for bubbles in the glass-to-metal or glass-to-glass seal. A series of bubbles that reduce the effective seal length to less than one external lead diameter shall be cause for rejection. Bubbles in the glass, but not effecting the glass-to-glass or glass-to-metal seal area, are not cause for rejection.

A.1.4 Glass package deformities (see figure 2074-A2). Any glass envelope deformity equal to or greater than 75 percent of the external lead diameter shall be cause for rejection.

A.1.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

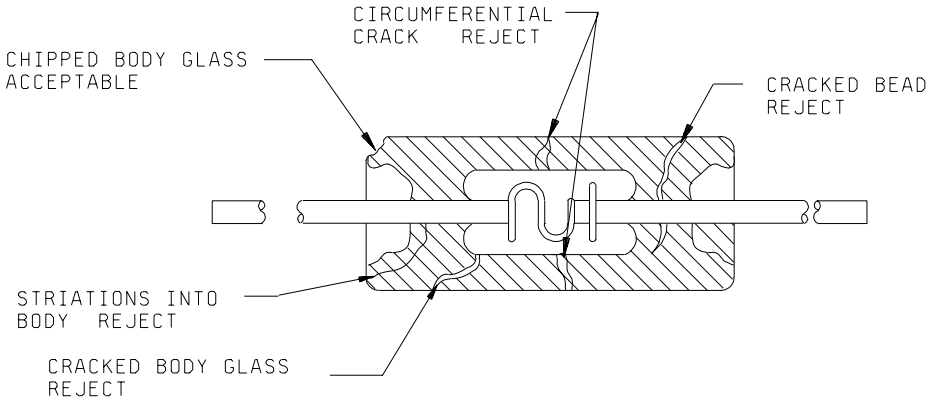
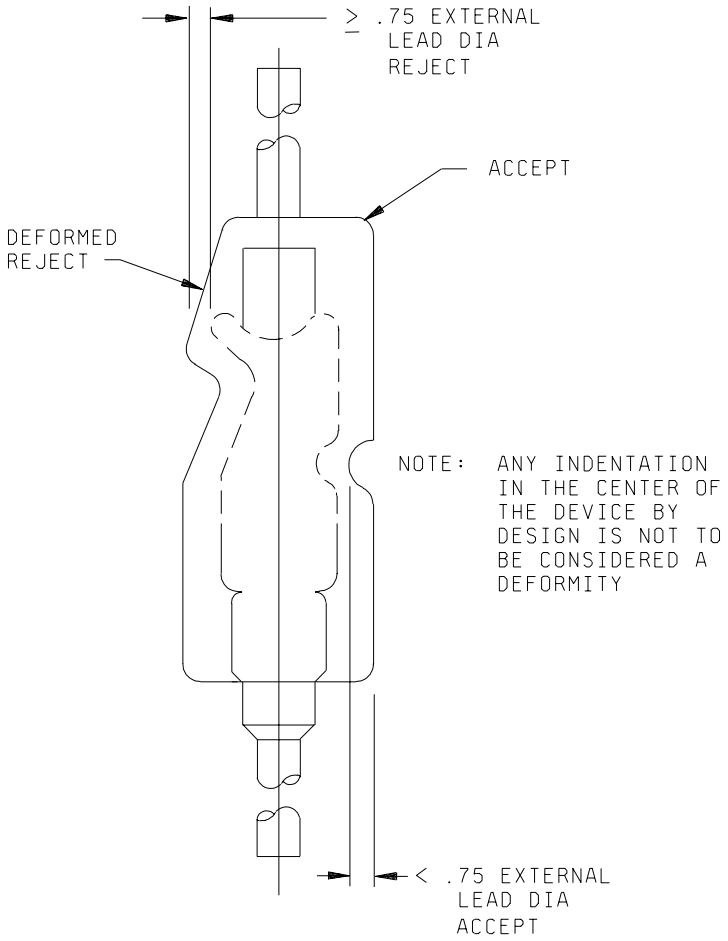


*FIGURE 2074-A1. Glass cracks and chips.

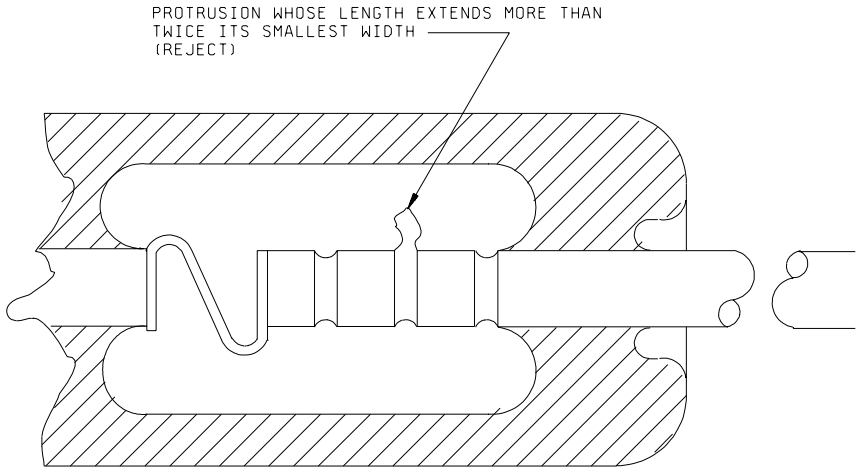
APPENDIX A



* FIGURE 2074-A2. Package deformities.

APPENDIX A

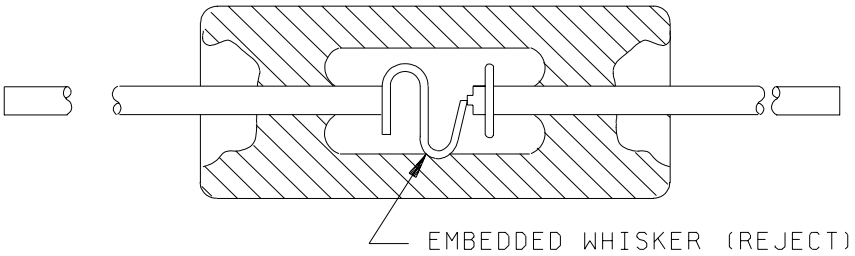
A.1.6 Solder protrusions (see figure 2074-A3). All devices shall be inspected for solder protrusions. Any device with a protrusion that extends more than twice the smallest protrusion width shall be rejected.



* FIGURE 2074-A3. Solder protrusions.

A.1.7 Pressure contact defects. The following misalignments or deformations shall be cause for rejection:

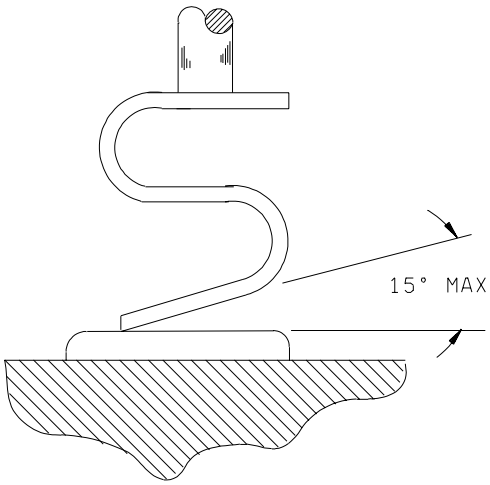
a. Whisker embedded within glass body wall (see figure 2074-A4).



* FIGURE 2074-A4. Embedded whisker.

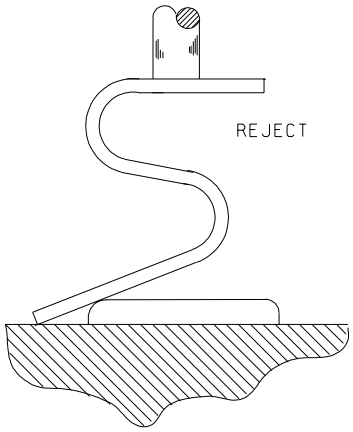
APPENDIX A

b. Toe contact between base of S or C spring and top surface of die caused by insufficient loading (see figure 2074-A5).



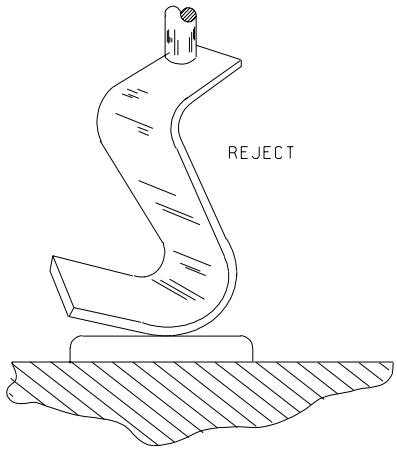
* FIGURE 2074-A5. Toe contact.

c. Toe contact on top surface of die (see figure 2074-A6).



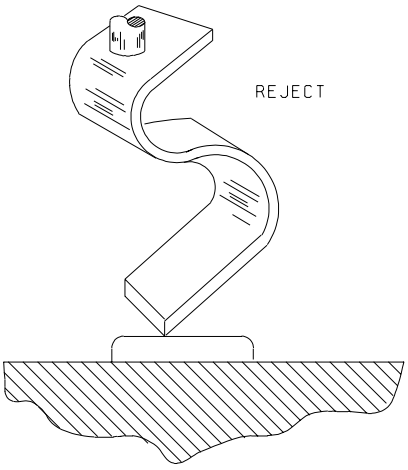
* FIGURE 2074-A6. Toe contact on top surface of die.

d. Heel contact between base of S or C spring and top surface of die (see figure 2074-A7).



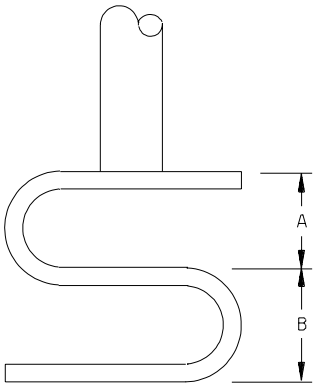
* FIGURE 2074-A7. Heel contact.

e. Point contact between base of S or C spring and top surface of die except by design (deformed or twisted whisker) (see figure 2074-A8).



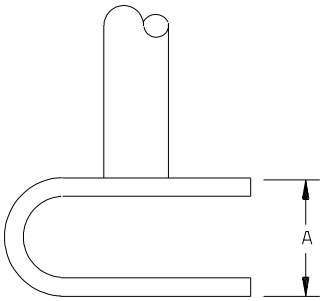
* FIGURE 2074-A8. Point contact.

f. Design compressed height (see figures 2074-A9 and 2074-A10). Either half of an S or C bend that is compressed so that any dimension is reduced to less that 50 percent of its design shall be rejected.



REJECT IF EITHER "A" OR "B" IS LESS THAN 50% OF ITS DESIGN COMPRESSED HEIGHT

* FIGURE 2074-A9. "S" whisker compressed height.



REJECT IF EITHER "A" IS LESS THAN 50% OF ITS DESIGN COMPRESSED HEIGHT

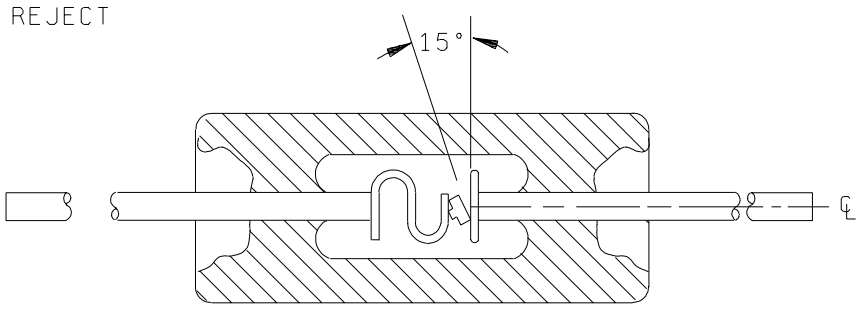
* FIGURE 2074-A10. "C" bend compressed height.

APPENDIX A

A.1.8 Whisker weld to post. Any device that exhibits weld splash or splatter (teardrop or balled) between whisker and post shall be rejected when it exceeds 25 percent of nominal lead diameter. The profile of the whisker weld to post shall not allow light penetration by more than 50 percent of lead diameter when using back lighting techniques.

A.1.9 Die to post or die to die contact area. Solder shall not be rough in appearance and shall be fused to a minimum of one-half the available bonding perimeter. Any solder overflow that touches the opposite surface of the die or dice shall be cause for rejection.

A.1.10 Die alignment (see figure 2074-A11). A device shall be rejected if the die surface is not within 15° of being normal to the centerline of the mounting post.



* FIGURE 2074-A11. Die alignment.

A.1.11 Lead alignment defects, (applicable to that portion of each lead within the glass envelope). A device lead which is either misaligned or bent so that it makes an angle with the principle device axis greater than 10 degrees shall be rejected.

A.1.12 Multiple chip attachment defects. A multiple chip stack that tilts more than 10 degrees from the principle axis of the device shall be cause for rejection.

APPENDIX B

SMALL SIGNAL, COMPUTER, REGULATOR, LOW POWER RECTIFIERS, AND MICROWAVE DIODES.

B.1 Axial lead transparent body straight through lead to die contact (see figure 2074-B1). The following criteria shall be specified for the straight through construction after encapsulation but before body coating or painting.

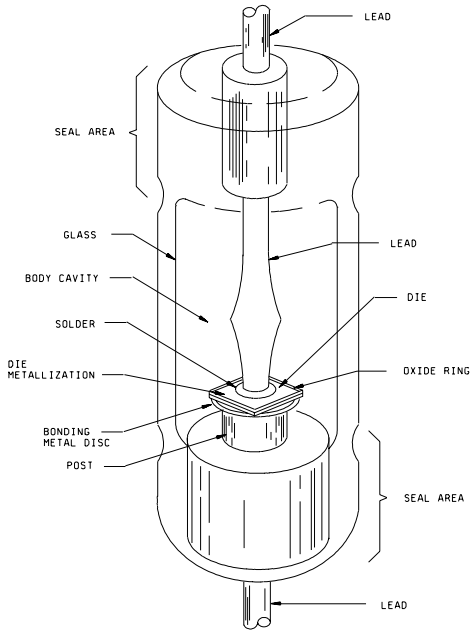
B.1.1 Glass cracks and chips (see figure 2074-A1). No cracks shall be allowed in the vicinity of the cavity. Any crack originating at either end of the package or crack that extends into the body of the glass toward the cavity more than 25 percent of the glass-to-glass or glass-to-metal seal length shall be cause for rejection. Any glass chip deep enough to expose the plug or lead surface and extending longitudinally into the glass-to-metal seal toward the cavity to reduce the effective seal length to less than one external lead diameter shall be cause for rejection.

B.1.2 Incomplete seal. All devices shall be inspected for glass-to-metal seal or glass-to-glass seal. Both seals shall be a minimum of one external lead diameter over the entire sealed portion (sealed interface).

B.1.3 Bubbles in seal. All devices shall be inspected for bubbles in the glass-to-metal or glass-to-glass seal. A series of bubbles that reduce the effective seal length to less than one external lead diameter shall be cause for rejection. Bubbles in the glass, but not effecting the glass-to-glass or glass-to-metal seal area, are not cause for rejection.

B.1.4 Glass package deformities (see figure 2074-A2). Any glass envelope deformity equal to or greater than 75 percent of the external lead diameter shall be cause for rejection.

B.1.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

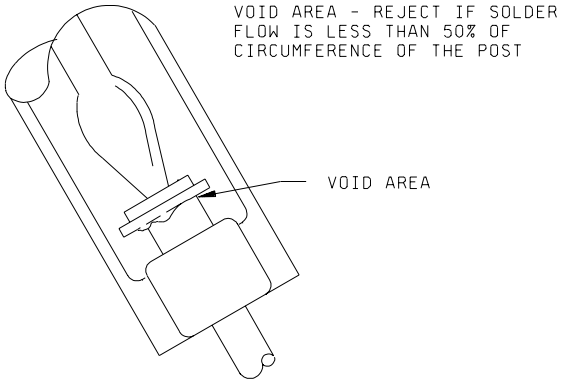


* FIGURE 2074-B1. Internal construction.

APPENDIX B

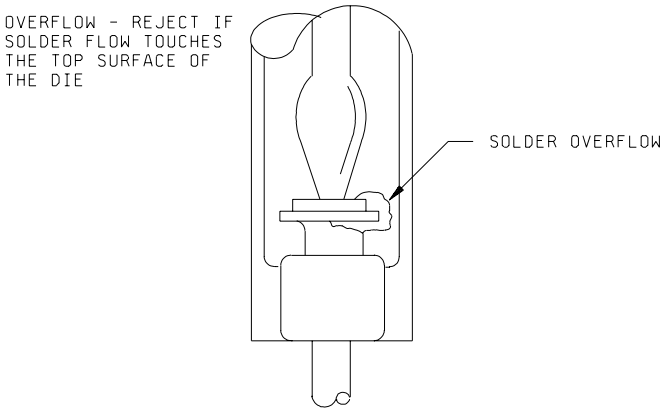
B.1.6 Die to post solder connection.

a. Solder voids (see figure 2074-B2). A device shall be rejected if solder flow is less than 50 percent of the perimeter of the minimum available contact area of the post.



* FIGURE 2074-B2. Solder voids.

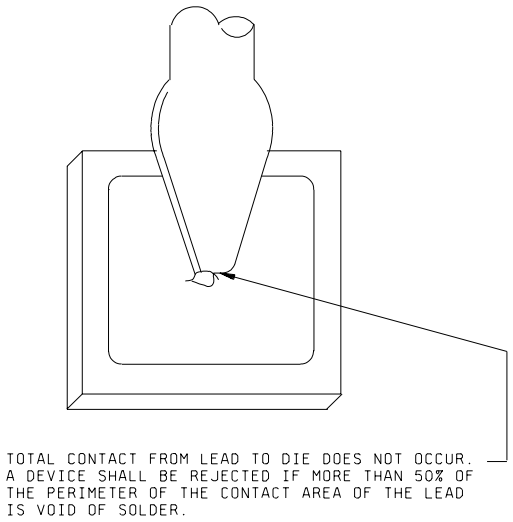
b. Solder overflow (see figure 2074-B3). A device shall be rejected if any solder flow touches the opposite surface of the die.



* FIGURE 2074-B3. Solder bridge.

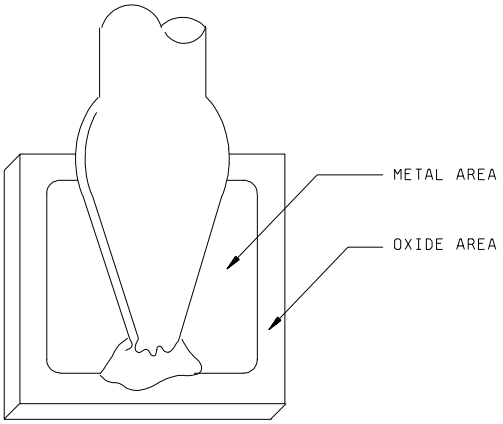
APPENDIX B

B.1.7 Lead to die solder connection (see figure 2074-B4). A device shall be rejected if more than 50 percent of the perimeter of the available contact area of the lead is void of solder.



* FIGURE 2074-B4. Solder voids.

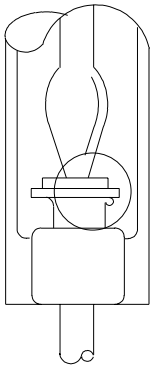
a. Solder overflow (see figure 2074-B5). A device shall be rejected if solder flow extends beyond 50 percent of the distance from the metal to the outer edge of the oxide.



* FIGURE 2074-B5. Solder overflow.

APPENDIX B

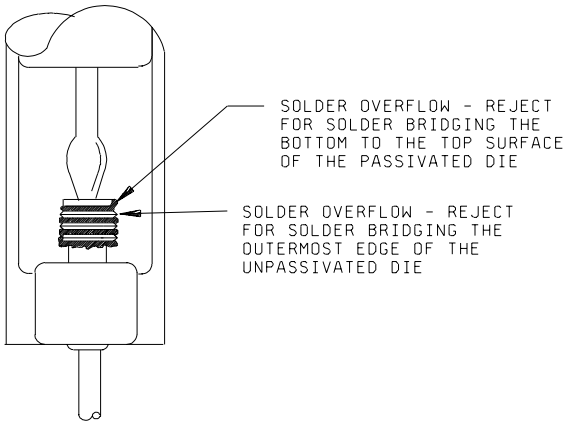
b. Solder protrusion, slivers, and spikes (see figure 2074-B6). A device shall be rejected if solder slivers and spikes are not securely attached to the main body. A securely attached sliver of spike is one having a cross sectional area greater at the area of attachment than anywhere else on the solder protrusion and having no necked down areas. Solder protrusions, slivers, and spikes whose length exceeds twice the smallest width of attachment shall be rejected.



* FIGURE 2074-B6. Solder slivers and spikes.

c. Solder balls. A device shall be rejected if there are any insecurely attached solder balls. An insecurely attached solder ball is one whose major cross sectional area is more than twice the cross sectional area of the attachment.

B.1.8 Die to die solder connection (see figure 2074-B7). A device shall be rejected if more than 50 percent of the perimeter of the available contact area of the die is void of solder.



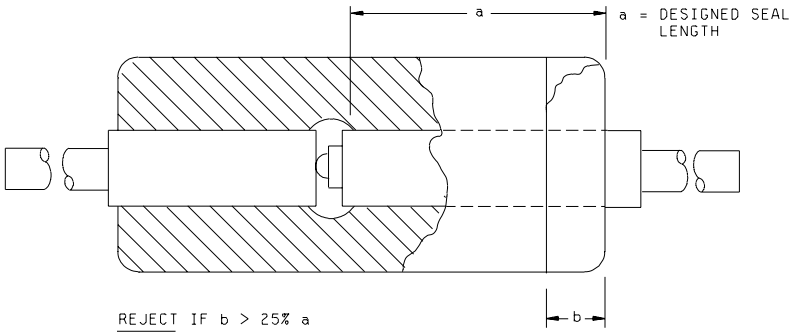
* FIGURE 2074-B7. Die to die solder connection.

APPENDIX C

* SMALL SIGNAL, COMPUTER, REGULATOR, LOW POWER RECTIFIERS, AND MICROWAVE DIODES

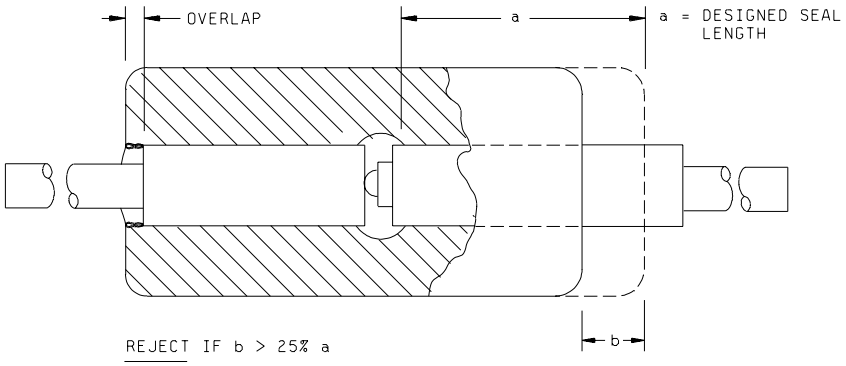
* C.1 Axial lead and surface mount, double plug, transparent body (, dumet plug, round end cap, soft glass).

C.1.1 Glass cracks (see figure 2074-C1). No cracks shall be allowed within 0.010 inch of the die. Any spiral or meniscus crack originating at either end of the package or glass that extends into the body of the glass toward the die more than 25 percent of the designed seal length shall be cause for rejection. Any chip deep enough to expose the plug surface and extending longitudinally into the glass toward the die more than 25 percent of the designed seal length shall be cause for rejection.



* FIGURE 2074-C1. Glass cracks.

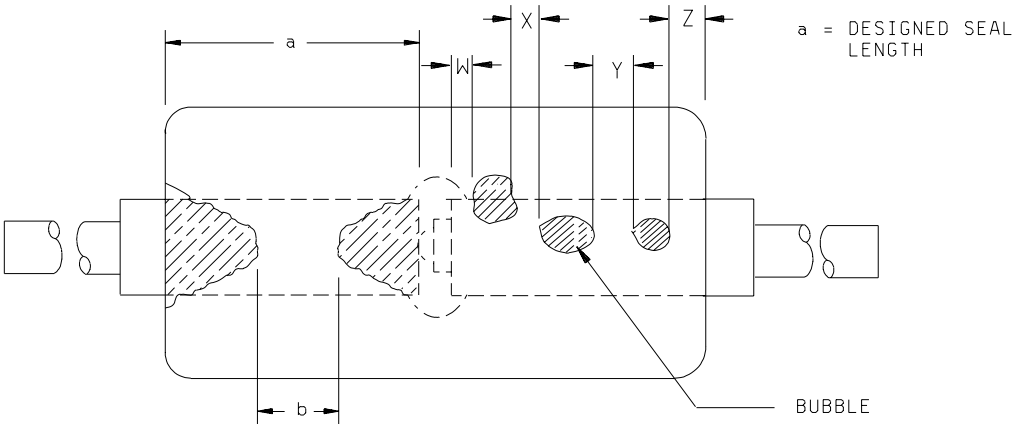
C.1.2 High seal (see figure 2074-C2). Any device which displays a glass case off center condition reducing the seal band of either plug by more than 25 percent of its designed length shall be cause for rejection.



* FIGURE 2074-C2. High seal.

APPENDIX C

C.1.3 Insufficient seal (see figure 2074-C3). Any anomaly such as bubbles, plug blisters, separations, leaching, or undersealing that affects the combined seal length of either plug by reducing the a sealing band to less than 50 percent of the designed seal length on any package type shall be cause for rejection.



* FIGURE 2074-C3. Insufficient seal.

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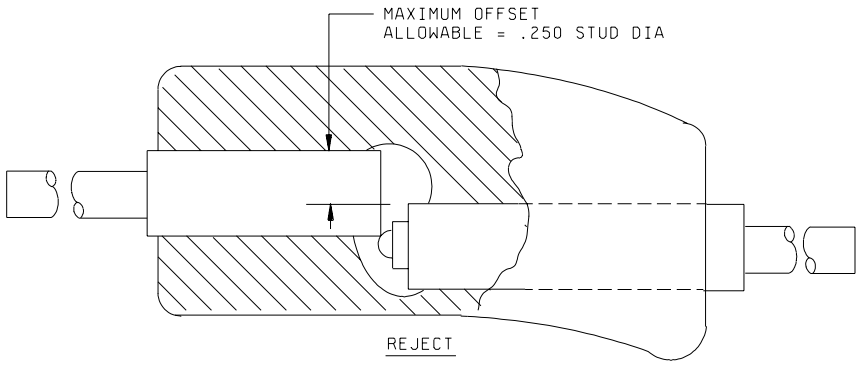
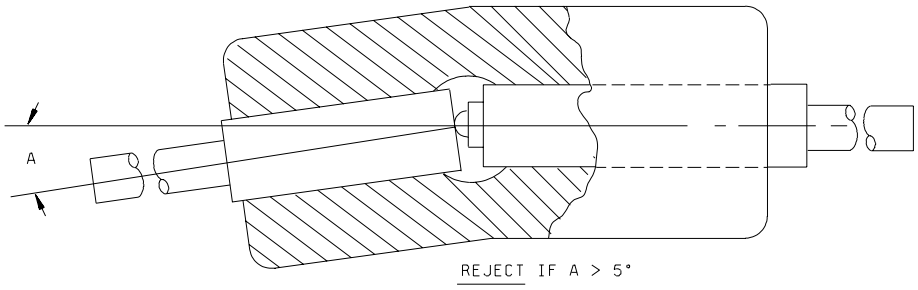
C.1.4 Plug alignment (see figures 2074-C4 and 2074-C5). All devices shall be inspected for proper plug alignment. A plug displacement distance more than 25 percent of the diameter of the plug shall be cause for rejection. The plug shall not tilt to the degree that it touches the chip or is misaligned from the other plug axis more than 5 degrees.



* FIGURE 2074-C4. Plug alignment.

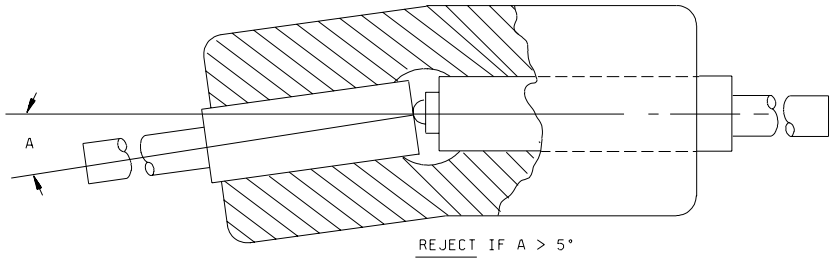


* FIGURE 2074-C5. Plug displacement.

C.1.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

APPENDIX C

C.1.6 Lead connections (see figure 2074-C6). Lead to plug connections shall be inspected for incomplete welds. Any partial welds less than 75 percent of total weld area shall be cause for rejection.



* FIGURE 2074-C6. Incomplete weld.

C.1.7 Die defects (reject).

C.1.7.1 Die tilt greater than 5 degrees or slug or preform makes contact to chip on bump side.

C.1.7.2 Any die that exhibits chip outs exceeding .25 inch (6.35 mm) the die width or extending to within 2 mils of the junction shall be rejected.

* C.1.8 Criteria for round end cap surface mount devices.

C.1.8.1 Glass to metal seal shall be .015 inch (0.381 mm) min for DO-213AA and .020 inch (0.508 mm) min for DO-213AB, around the diameter of each slug.

C.1.8.2 Slug exposure shall not exceed 30 percent of the slug length (.014 inch (0.3556 mm) min for DO-213AA and .022 inch (0.5588 mm) min for DO-213AB).

C.1.8.3 There shall be no cracks in the device within .010 inch (0.254 mm) of the die.

C.1.8.4 There shall be no cracks in the glass that are pointed towards the die.

C.1.8.5 There shall be no conductive contaminants in the die cavity area.

C.1.8.6 For plug alignment, including end caps, see C.1.4.

C.1.8.7 For end cap connections, see C.1.6.

APPENDIX D

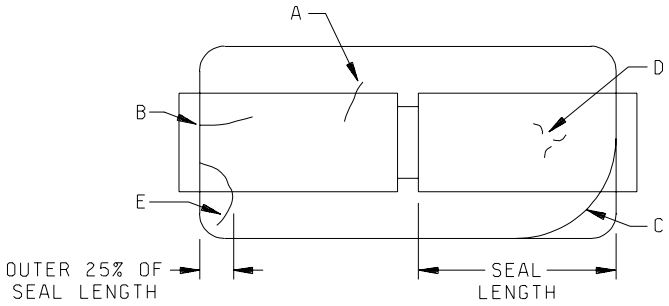
* (ALL, COMPUTER, REGULATOR, RECTIFIER, AND MICROWAVE DIODES)

* D.1.0 Axial lead and surface mount double plug, transparent body (tungsten or molybdenum plug, square end cap, hard glass).

* D.1.1 Glass.

* a. Cracks. Spiral or longitudinal cracks of any length originating at either end that propagate in the direction of the die are cause for rejection. Reject for cracks that are not confined to the glass surface or the outer 25 percent of the seal length. Cracks confined to the outer 25 percent of the designed seal length that propagate back toward the starting edge (away from the die area) are acceptable. Small surface impact marks, "c" cracks and microcracks are acceptable if they are confined to the glass surface with no other cracks radiating from them are acceptable. (Figure 2075-D1.)

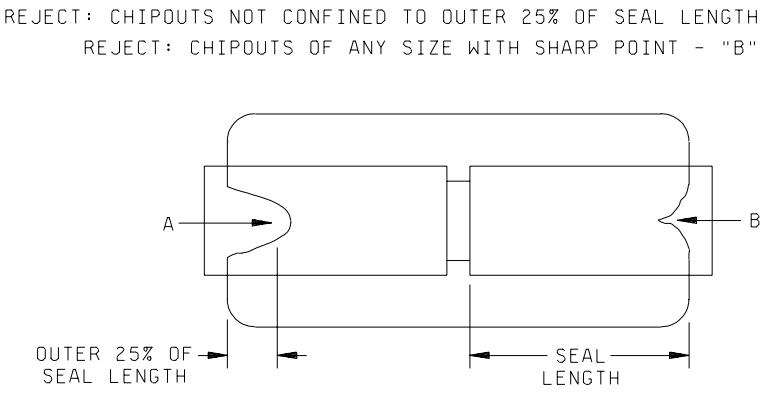
REJECT: CRACKS NOT CONFINED TO SURFACE OR OUTER 25% OF SEAL LENGTH - "A"
REJECT: CRACKS OF ANY LENGTH THAT PROPAGATE TOWARD DIE - "B"
REJECT: SPIRAL CRACKS PROPAGATING TOWARD DIE - "C"
ACCEPT: SMALL C-CRACKS OR MICRO CRACKS IN GLASS SURFACE - "D"
ACCEPT: CRACKS IN OUTER 25% OF SEAL LENGTH THAT PROPAGATE AWAY FROM DIE - "E"



* FIGURE 2074-D1. Cracks.

APPENDIX D

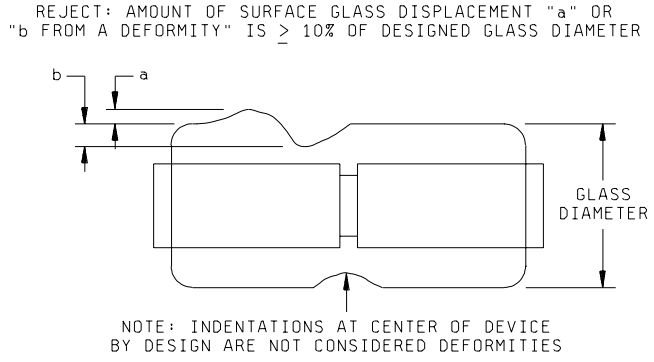
* b. Chipouts. Edge chipouts that expose a plug and are not confined to the outer 25 percent of the designed seal length are cause for rejection. Edge chipouts (regardless of size) that expose a plug and create a sharp angle or “V” shape that points toward the die area are rejects (Figure 2074-D2).



* FIGURE 2074-D2. Chipouts.

* c. Holes. Any hole over the die or slug area greater that 50 percent of the glass thickness in depth is cause for rejection except that holes of any depth are acceptable in the outer 25 percent of the designed seal length.

* d. Deformities. Any glass surface deformity that causes the glass surface to be displaced by more than 10 percent of the designed glass diameter or that results in the device not meeting a dimensional requirement is cause for rejection. (Figure 2074-D3.)

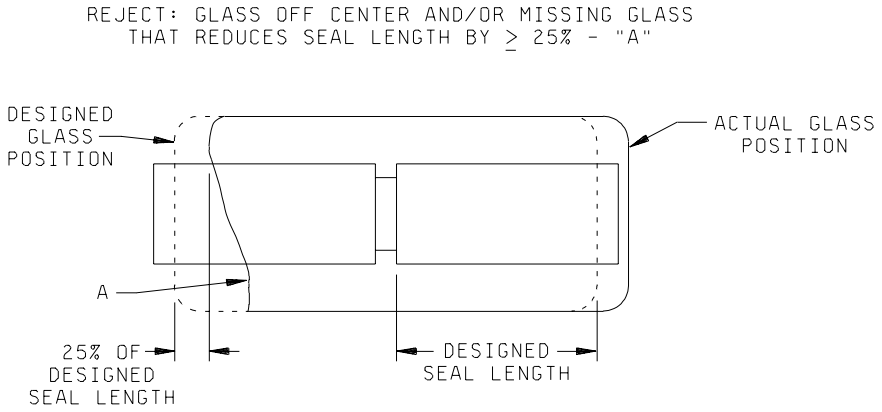


* FIGURE 2074-D3. Deformity.

* e. Surface damage and discoloration. Any device with surface abrasions, chips, scratches, rough or discolored (darkened) glass over the die area that result in the die not being clearly visible is a reject. Using liquid immersion to improve die visibility is acceptable.

D.1.2 Seal.

* a. Glass positioning and missing glass. Off center glass and/or portions of missing glass that reduce the seal length on either plug by more than 25 percent of the designed seal length is cause for rejection. (Figure 2074-D4.)



* FIGURE 2074-D4. Positioning.

* b. Insufficient seal. Seal surface anomalies such as undercut, separations, plug blisters, scratches or cracks, bubbles, silicon chips, fibers, or missing plating which, when combined, reduce the sealing length along any linear path to less than 50 percent of the designed seal length are cause for rejection. NOTE: Lines or "strings" of small bubbles are considered to be seal anomalies for the entire length of the line. (Figure 2074-D5.)

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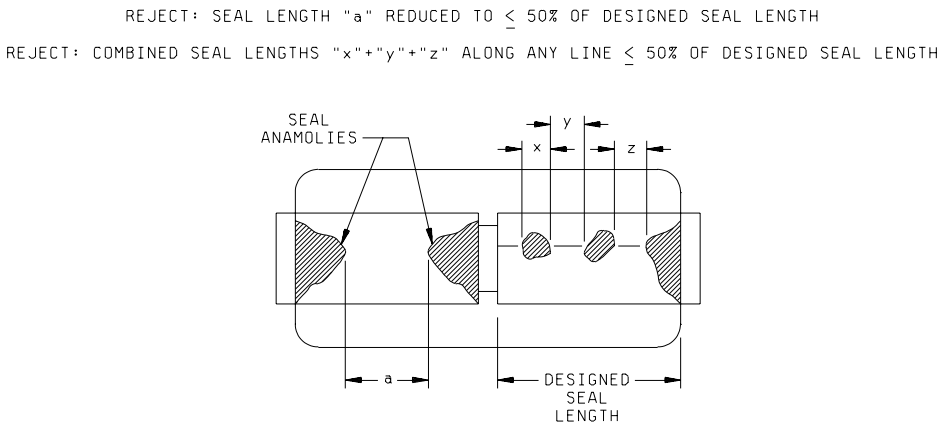
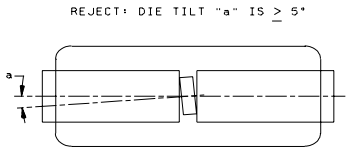


* FIGURE 2074-D5. Insufficient seal.

* c. Extraneous or loosely attached materials. Any unattached or loosely attached solder, braze, silicon chips, flaked plating, fibers or other opaque extraneous material in the die cavity (for cavity devices) that is greater than 1 mil in any dimension are cause for rejection. No solder, braze or other bonding materials shall extend from a plug into the area between plugs.

D.1.3 Alignment. NOTE: Any die to plug non-contact that occurs as a result of die or plug misalignment is most accurately evaluated by thermal impedance testing. In cases where pass/fail status of a device is unclear based on the alignments requirements presented herein, thermal impedance testing may be used to determine the acceptability of the device.

* a. Die alignment: Any die that tilts more than 5 degrees with respect to the surface of either plug or that tilts sufficiently to make any unintended contact with the plug is cause for rejection. (Figure 2074-D6.) Any die that is out of axial alignment such that it extends beyond the slug more than 20 percent of its length or width is cause for rejection. (Figure 2074-D7)



* FIGURE 2074-D6. Tilt.

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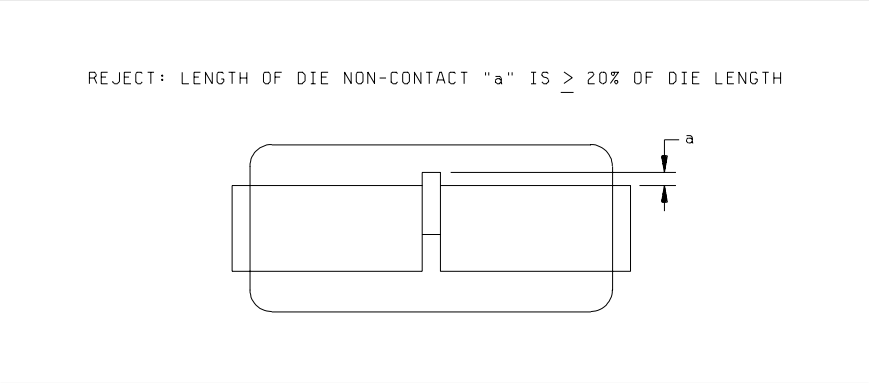
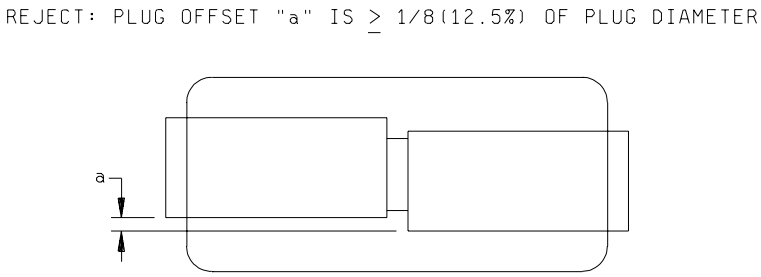


* FIGURE 2074-D7. Die non-contract.

* b. Plug alignment. Plugs that are not axially aligned other in the die area to within 1/8 (12.5 percent) of the diameter of the plug are cause for rejection. (Figure 2074-D8.) Any plug that tilts more than 5 degrees with respect to the other or that tilts sufficiently to make any unintended contact with the die is cause for rejection (Figure 2074-D9).



* FIGURE 2074-D8. Plug offset.

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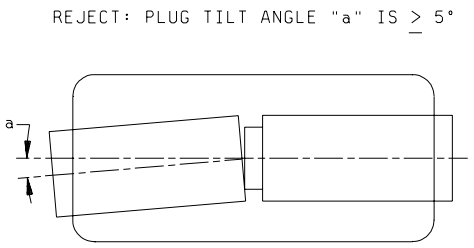
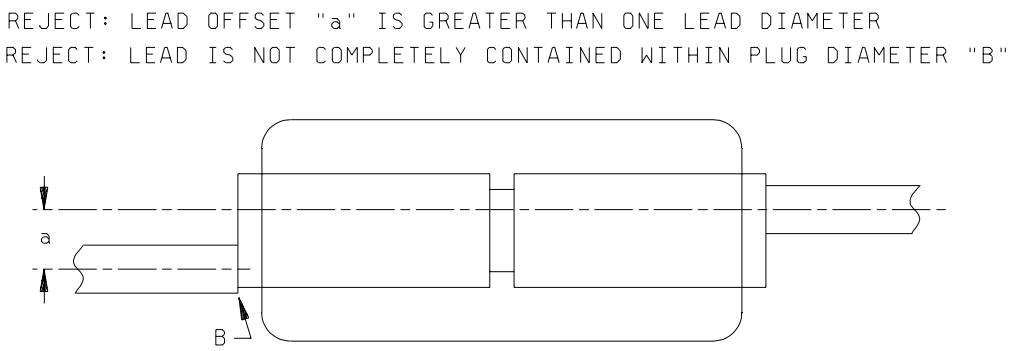


* FIGURE 2074-D9. Plug tilt angle.

D.1.4 Lead and end cap attach.

* a. Lead alignment (leaded devices). Leads that are not axially aligned to within one lead diameter or leads that are not contained completely within the diameter of the plug are cause for rejection (Figure 2074-D10).



* FIGURE 2074-D10. Lead offset.

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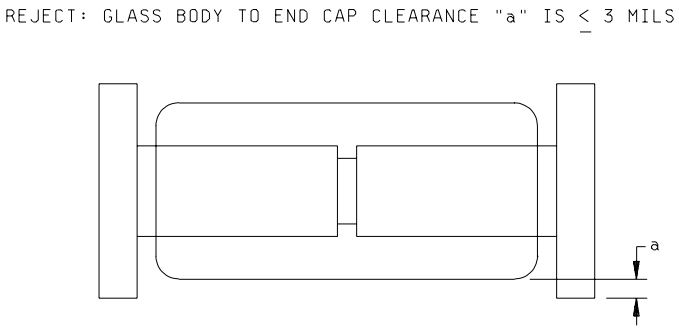
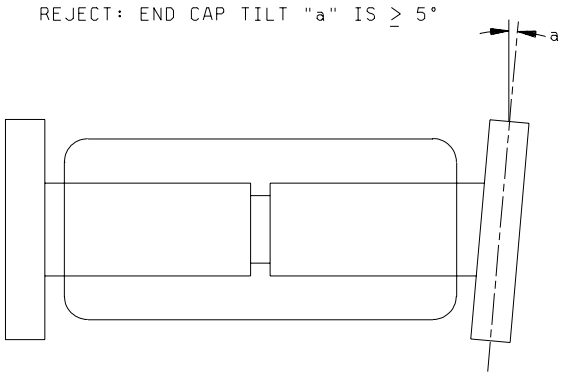
* b. Braze (leaded devices). Leads that are not brazed to the plug around at least 90 percent of the lead perimeter are cause for rejection. Any cracks or fissures in the braze are cause for rejection. Pin holes in the braze are acceptable.

* c. End caps (surface mount). Reject for end caps that do not allow at least 3 mils clearance from the glass body to the mounting surface on all four sides (Figure 2074-D11). Reject for end caps that are not perpendicular to the plugs to within 5 degrees (Figure 2074-D12). Reject for end caps that are bent sufficiently to cause the device to exceed any specified diode or end cap dimension (Figure 2074-D13). Reject for end cap rotation where mounting surfaces are not co-planer to each other to within 5 degrees (Figure 2074-D14). Reject for tabs that have indentations, holes or other damage effecting more than 25 percent of any mounting surface (Figure 2074-D15). Reject for end caps that exhibit flaking, blistering or peeling.



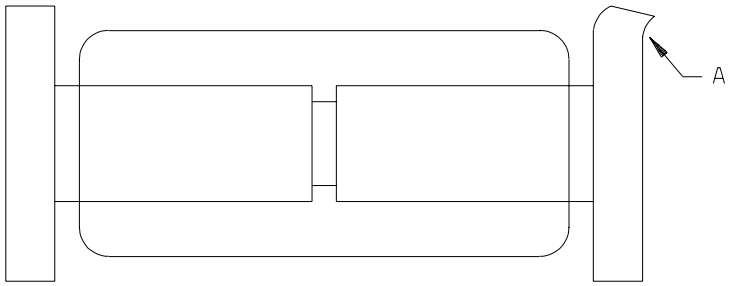
* FIGURE 2074-D11. End cap clearance.



* FIGURE 2074-D12. End cap tilt.

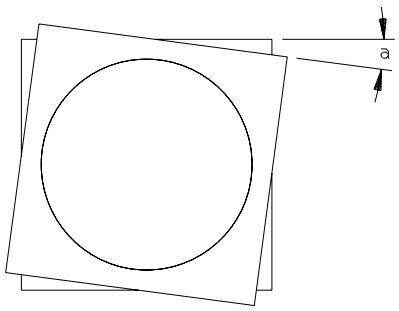
APPENDIX D

REJECT: DEVICE WITH END CAP DEFORMATION THAT EXCEEDS ANY SPEIFIED DEMENSION - "A"



* FIGURE 2074-D13. End cap deformation.

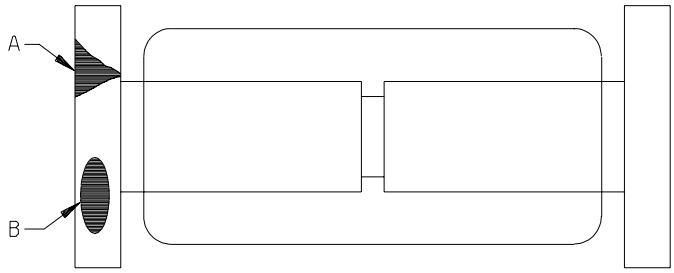
REJECT: END CAP ROTATION "a" $\geq$ 5°



* FIGURE 2074-D14. End cap rotation.

APPENDIX D

REJECT: ANY MOUNTING SURFACE REDUCED TO $\leq$ 75%
OF IT'S DESIGNED AREA DUE TO NICKS("A"), PITS("B"),ECT.



* FIGURE 2074-D15. Nicks.

APPENDIX E

SMALL SIGNAL, COMPUTER, REGULATOR, LOW POWER RECTIFIERS, AND MICROWAVE DIODES

E.1 Axial lead, transparent body, point contact. The following additional criteria shall be specified for the point contact construction after encapsulation but before body coating or painting.

E.1.1 Glass cracks and chips (see figure 2074-A1) No cracks shall be allowed in the vicinity of the cavity. Any crack originating at either end of the package or crack that extends into the body of the glass toward the cavity more than 25 percent of the glass-to-glass or glass-to-metal seal length shall be cause for rejection. Any glass chip deep enough to expose the plug or lead surface and extending longitudinally into the glass-to-metal seal toward the cavity to reduce the effective seal length to less than one external lead diameter shall be cause for rejection.

E.1.2 Incomplete seal. All devices shall be inspected for glass-to-metal seal or glass-to-glass seal. Both seals shall be a minimum of one external lead diameter over the entire sealed portion (sealed interface).

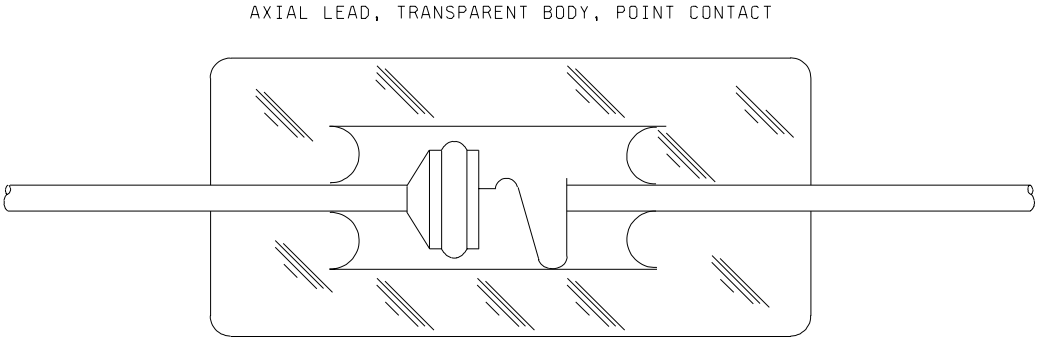
E.1.3 Bubbles in seal. All devices shall be inspected for bubbles in the glass-to-metal or glass-to-glass seal. A series of bubbles that reduce the effective seal length to less than one external lead diameter shall be cause for rejection. Bubbles in the glass, but not effecting the glass-to-glass or glass-to-metal seal area, are not cause for rejection.

* E.1.4 Glass package deformities (see figure 2074-A2). Any glass envelope deformity equal to or greater than 75 percent of the external lead diameter shall be cause for rejection.

E.1.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

E.1.6 Pressure contact defects. The following misalignments or deformities shall be cause for rejection:

a. Whisker touches glass body wall (see figure 2074-E1).



* FIGURE 2074-E1. Whisker touches glass body wall (reject).

b. Whisker loops touch one another (see figure 2074-E2).

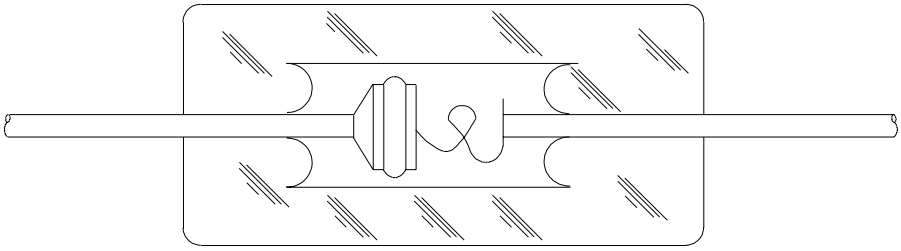


*FIGURE 2074-E2 . Whisker loops touch one another (reject).

c. Whisker angle over 10 degrees from normal (see figure 2074-E3).

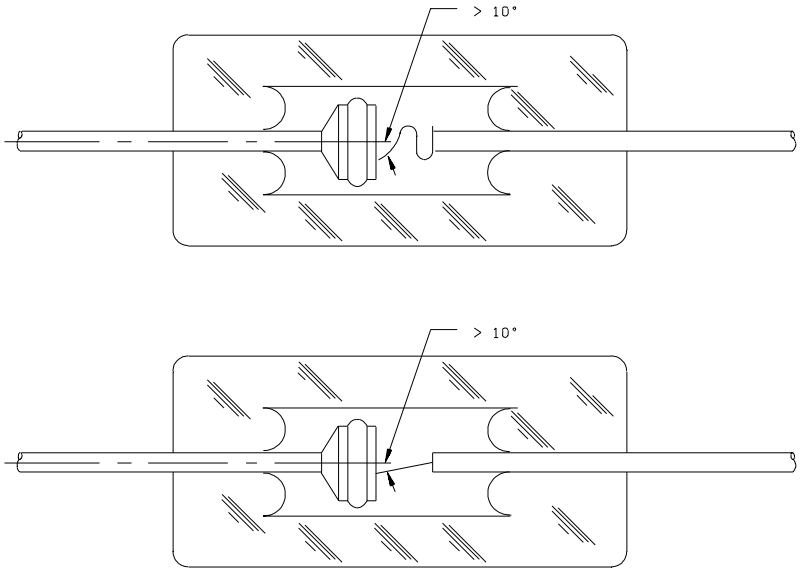


*FIGURE 2074-E3 . Whisker angle over 10 degrees from normal (reject).

APPENDIX E

E.1.7 Whisker weld to post. Any device that exhibits weld splash or splatter (tear dropped or balled) between whisker and post shall be rejected when it exceeds 25 percent of nominal lead diameter. The profile of whisker weld to the post shall not allow light penetration by more than 50 percent of lead diameter when using back lighting techniques.

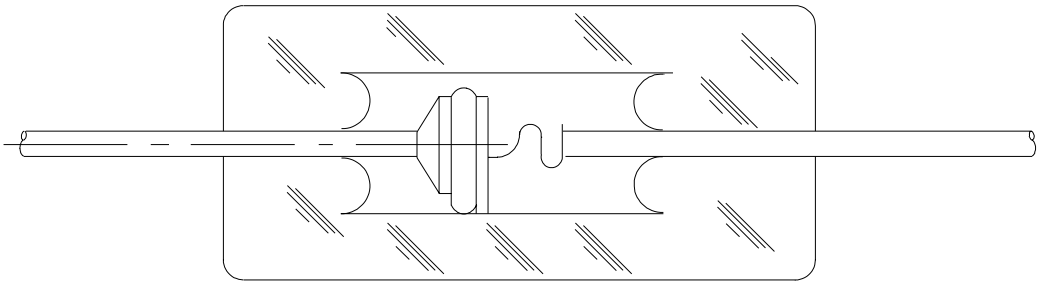
E.1.8 Solder voids. A device shall be rejected if solder flow is less than 50 percent of the perimeter of the minimum available contact area of the die.

E.1.9 Die to post contact area. Solder shall be smoothly formed from one element to another and shall be fused to a minimum of one-half the available bonding area. Any solder overflow that touches the opposite surface of the die shall be cause for rejection.

E.1.10 Die alignment. A device shall be rejected if the die surface is not within 15° of being normal to the centerline of the mounting post.

E.1.11 Lead alignment defects (applicable to that portion of each lead within the glass envelope). A device whose lead is either misaligned or bent so that is makes an angle with the principle device axis greater than 10° shall be rejected.

E.12 Die touches glass package (see figure 2074-E4). A device shall be rejected if the die touches the glass envelope.



* FIGURE 2074-E4. Die touches glass package (reject).

APPENDIX F

POWER RECTIFIERS AND REGULATORS

F.1 Axial lead double plug opaque body.

F.1.1 Die mounting and alignment. After bonding die to the heat sink, plugs, or leads, the following shall be inspected for defects:

a. Die geometry. A die shall be rejected if it is chipped or broken to the extent that 75 percent or less of the original surface remains.

b. Axial alignment of plugs and die. Plugs shall be aligned axially within one-eighth of the diameter of either plug.

c. Tilted die. A device shall be rejected if the die is tilted so that the die surface is greater than 5 degrees from being perpendicular to the mounting post axis.

F.1.2 Die cracks. Any die exhibiting cracks that reduce the total die area (or cracks extending into or across the junction area) to less than 75 percent of its original area shall be cause for rejection.

F.1.3 Inadequate brazing. A device shall be rejected if less than 90 percent of the visible metallized surface (perimeter) is brazed to the heat sink or lead.

F.1.4 Flaking or loose material. No unattached solder, braze, or other bonding material shall extend from the plugs. Any blistering or peeling of plug surface shall be cause for rejection.

F.1.5 Extraneous matter. A device shall be rejected if there is any extraneous, particulate matter between the terminal plugs or on the plug surface. No foreign stains shall be permitted on plug surfaces.

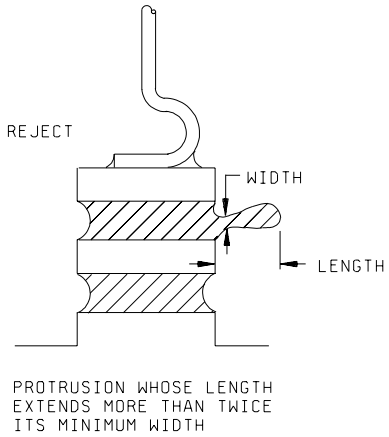
APPENDIX G

SMALL SIGNAL, COMPUTER, REGULATOR, LOW POWER RECTIFIERS, AND MICROWAVE DIODES

G.1. Axial lead, metal body, solder contact design.

* G.1.1 Examinations before capping.

*a. Solder defects (see figures 2074-G1 and 2074-G2). Any device with a solder protrusion that extends more than twice the smallest protrusion width shall be rejected. Solder shall be smoothly formed from one element to another and shall be fused to a minimum of 50 percent of the perimeter between adjacent elements.



* FIGURE 2074-G1. Solder protrusion.

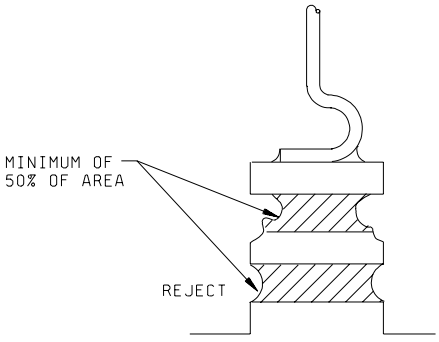


FIGURE 2074-G2. Solder flow.

APPENDIX G

*b. Alignment (see figure 2074-G3). Any device whose element has its geometric center displaced more than 33 percent of its width from the die or die stack centerline shall be rejected.

*c. Tilt (see figure 2074-G4). Any element of a device that is tilted more than 10 degrees from the mounting plane shall be cause for rejection.

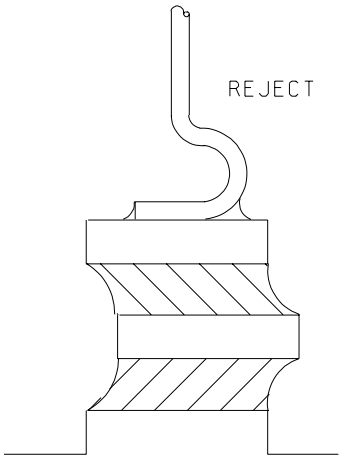
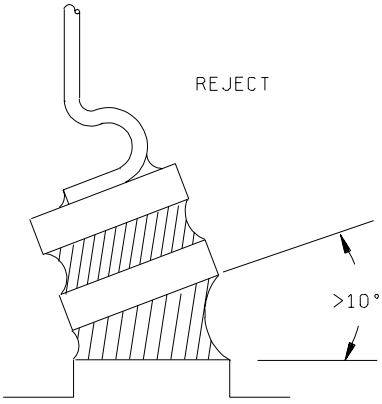


*FIGURE 2074-G3. Element alignment.



* FIGURE 2074-G4. Element tilt.

*d. Die chipouts (see figure 2074-G5). Any device die that exhibits chipouts extending more than 25 percent of the die width or to within 2 mils of the junction area shall be cause for rejection.

*e. Die cracks (see figure 2074-G6). Any die exhibiting cracks that reduce the total die area (or cracks extending into or across the junction area) to less than 75 percent of its original area shall be cause for rejection

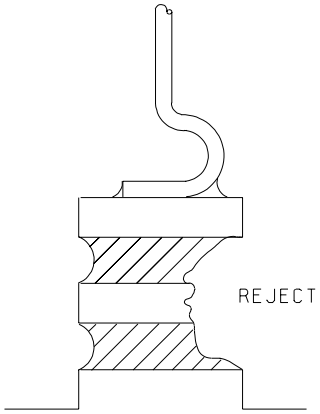


*FIGURE 2074-G5. Die chipout.

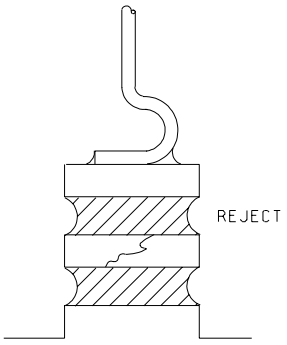


*FIGURE 2074-G6. Die cracks.

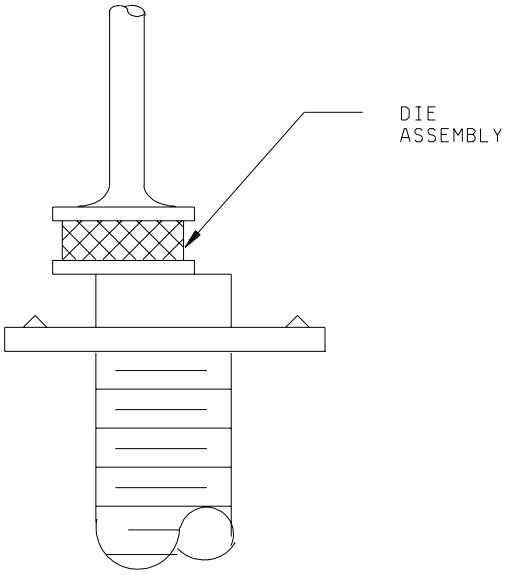
f. Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

APPENDIX H

POWER RECTIFIERS AND REGULATORS

H.1 Metal body stud mounted devices. The following inspections shall be made prior to capping.

* H.1.1 Die and lead assembly (see figures 2074-H1 and 2074-H2). The die and lead assembly shall be located on the base pedestal so that there is complete contact over the design contact area. The lead shall be free of nicks and scrapes that reduce the lead diameter by more than 5 percent. The die and lead assembly shall not be tilted more than 5 degress with respect to the base.



* FIGURE 2074-H1. Offset die.

APPENDIX H

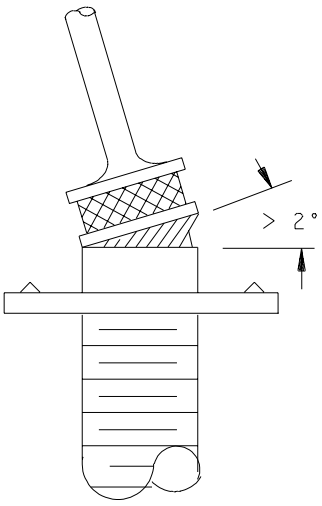


*FIGURE 2074-H2 . Tilted die.

* H.1.2 Extraneous matter.

a. Solder slivers and spikes. A device shall be rejected if solder slivers and spikes are not securely attached to the parent body of the solder. A securely attached sliver or spike is one having a cross sectional area greater at the area of attachment than anywhere else on the solder protrusion and having no necked-down areas.

b. Foreign matter. A device shall be rejected if there are unattached solder balls, semiconductor materials, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

c. Multiple die attachments. A device shall be rejected if the attached portion of an adjacent die exceeds 25 percent of the die area.

* H.1.3 Assembly defects.

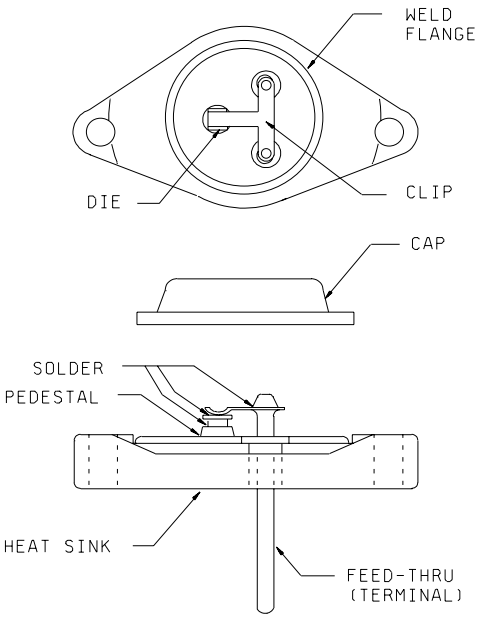
a. Tilted elements. A device shall be rejected if any element of the assembly is tilted in excess of 10E from the normal mounting plane.

b. Misaligned elements. A device shall be rejected if any element of the assembly is misaligned or displaced in excess of 33 percent of its width from the die or die stack centerline, bridges two active regions, or extends beyond the isolation region of the oxide.

APPENDIX I

POWER RECTIFIERS AND REGULATORS

* I.1 Metal body diamond base regulators (see figure 2074-I1).



* FIGURE 2074-I1 . Diamond base construction.

* I.1.1 Die to pedestal and die to clip solder connections.

a. Solder voids. A device shall be rejected if solder flow is less than 50 percent of the perimeter of the minimum available contact area.

b. Solder overflow. A device shall be rejected if any solder flow bridges from the top to bottom surface of the die or reduces the normal separation of two active regions by 50 percent or more.

* I.1.2 Clip to post and feed through to heat sink solder connections.

a. Solder voids. A device shall be rejected if the wetting action of the solder to each member of the connection is not continuous.

b. Solder overflow. A device shall be rejected if any solder flow extends on to any portion of the weld flange of the heat sink.

METHOD 3100

JUNCTION TEMPERATURE MEASUREMENT AT BURN-IN & LIFE TEST

1. Purpose. This test is conducted on a representative sample of devices to verify a desired junction temperature ($T_{J)}$ is achieved during burn-in and life-test environments. There are two methods that may be used. Both use a temperature sensitive parameter (TSP) that is initially measured at the desired T_J and selected test-current levels. In the first test method A, a selected low measuring current that does not cause significant self-heating is used (similar to thermal resistance test methods). In the second test method B, a series of sequential current pulses are taken to characterize the TSP at the desired T_J in the same operating current region expected for the burn-in and life-test environments. These TSP values are again later compared during burn-in or life-test to verify the same T_J. In either case, a direct sampling method of T_J in the burn-in or life test environment minimizes or eliminates possible errors introduced by ambient conditions, K factor, and non-linearity of component thermal resistance when applied at high temperatures. The method also allows the burn-in and life-test environment to be accurately characterized for thermal resistance junction to ambient ($R_{\theta JA}$) that can be used again to further advantage for similar products in the same test environment.

2. Scope. This applies to diode and transistor bipolar products requiring junction temperature verification during power burn-in that generates self-heating of T_J well above ambient or case temperature with applied power. It may also use an oven chamber or hot plate for achieving elevated ambient or case temperatures. The applied power testing may include ac operating life (ACOL) conditions for rectifiers, dc power in the operating breakdown region for zeners, and forward dc power conditions for signal diodes and others. Transistors also involve applied dc power conditions. This generally does not apply to high temperature reverse bais (HTRB) unless sufficient power is applied to cause significant self-heating. Equivalent heating power options are also described in method A to accommodate existing TSP equipment measurement methods for thermal resistance.

3. Rationale. Increased requirements for semiconductor performance, reliability, and quality have forced the need for knowledge and greater accuracy of semiconductor device junction temperatures at burn-in and life testing. This is necessary for making long-term calculations for reliability levels if using accelerating effects of burn-in or life testing. Accurate T_J measurements can be difficult because of the many variables. Electrical considerations (power, voltage-current levels, waveforms, etc), environmental consideration (mounting configuration, surroundings, mounting methodology, etc.) and selection of the junction temperature sensing method will affect results. It should also be noted that the thermal resistance characteristics of any semiconductor device are not necessarily constant with temperature or power dissipation, thus requiring thermal measurements under conditions that best duplicate actual operation in the burn-in or life-test environment for determining T_J.

4. Definitions. Many features are identical to those used for measuring thermal resistance for test method A. For both methods, the burn-in and life test environment shall simply be known as the “test environment.” Further details may be found in other references including EIA-531, JESD51-1, and methods 3101, 3131, and 4081 of MIL-STD-750.

a. TSP — Temperature sensitive parameter at the measuring current.

b. T_J — Junction temperature.

c. T_A — Ambient temperature in the test environment.

d. $R_{\theta JA}$ — Thermal resistance from junction to ambient.

e. $R_{\theta JL}$ — Thermal resistance from junction to lead.

f. $R_{\theta JC}$ — Thermal resistance from junction to case.

g. $R_{\theta JEC}$ — Thermal resistance from junction to end cap.

h. I_M Measuring current for the TSP (V_F or V_{BE}).

i. I_H Heating current.

j. t_H Heating time.

k. t_{MD} Measurement delay time

l. P_H Heating power.

m. V_F Forward voltage.

n. V_{BE} Base-emitter voltage.

o. V_{CE} Collector-emitter voltage.

p. I_C Collector current.

q. I_B Base current.

r. $V_{(BR)}$ Breakdown voltage.

s. V_Z Zener voltage.

t. I_F Forward current.

u. I_O Average I_F for 50 or 60 Hz sine wave and 180 degree conduction angle.

v. I_R Reverse standby current.

w. EC End cap.

x. DUT Device under test.

5. Equipment. Applicable to both methods unless otherwise noted.

5.1 TSP measurement. Test equipment to initially measure the TSP in a controlled temperature chamber, bath, or hot plate is required at a desired T_J for sample DUT.

5.2 Power supplies and arrays. The equipment used shall also include the burn-in or life-test power supplies and panel/socket arrays for electrical contacts or heat sinking where the T_J is to be sample measured for the DUTs. This "test environment" is the same as used for all other remaining devices intended for burn-in screening or life test.

5.3 Oven chamber. An oven chamber, bath, or hot plate to place the panel socket arrays with all the devices shall be used if elevated ambient temperatures are required.

5.4 Measuring TSP. For test method A, equipment for measuring the TSP shall be similar to that described for thermal resistance in EIA-531, JESD51-1, TM3101, TM3131, or TM4081. The TSP is sampled in a short measurement delay time (t_{MD}) after switching to a low measuring current I_M from the applied heating power source. The duty factor for sampling the TSP shall be 1percent or less of the heating time (t_H). It is considered optimum to use the same mode of power or heating current (I_H) as the power used in the test environment conditions. However, this method also allows for a dc forward heating current (I_H) power source often used in thermal resistance test methods to provide equivalent rms power.

5.5 Sample-and -hold tester. For test method B, a sample-and-hold tester for recording a sequential set of TSP measurements at operating currents in the same vicinity as the test environment operating current is required such as a Frothingham VF40 or equivalent with the approval of the quality activity. The test pulses must be kept narrow and widely spaced where additional heating of the junction will be insignificant.

5.6 Voltage and current measurements. In test method B, a voltmeter and current meter shall be used to accurately measure the expected voltage and current levels in the test.

5.7 Thermocouple. A small bare-wire thermocouple of 36 AWG is required for ACOL evaluation.

6. Procedure for method A. This method uses a selected low measuring current for the TSP that does not cause significant self-heating (similar to thermal resistance test methods). The DUTs are a sample of serialized devices where the TSP is initially recorded at the desired temperature. They shall also be of the same construction as other devices in the "test environment" and be of sufficient quantity to provide a good sample for averaging. Unless otherwise specified, this shall be a minimum of five devices.

6.1 TSP measurement. First determine the nominal T_J desired for the burn-in or life test. For military burn-in screening, the minimum T_J shall be specified by the applicable detail spec. The maximum T_J is the rating for the DUT unless otherwise specified.

6.1.1 Desired T_J. In a separate temperature controlled chamber, bath, or hot-plate environment, the nominal T_J desired for the burn-in or life test will initially be established within plus or minus 2°C (or as required) for recording the TSP. Additional T_J tolerance considerations are also noted in step 6.3.3.

6.1.2 Recording TSP. After the DUTs have been introduced and brought to thermal equilibrium, the TSP shall be recorded in a serialized manner at a low steady-state-measuring current (I_M) for method A. This would be the forward voltage of a diode (V_F) or base-emitter voltage (V_{BE}) of a transistor. The magnitude of I_M shall be large enough to ensure the V_F or V_{BE} is turned on, but not large enough to cause significant self-heating. For transistors, it is optimum to remove any bias voltage to the collector that generates current gain affecting I_M. However some thermal resistance equipment requires use of a collector voltage for a V_{BE} measurement. If so, that same test condition shall be used for measuring the TSP in burn-in as described in 6.3.2 and 6.4.1e.

6.2 Test environment mounting.

6.2.1 Verifing T_J. The sample DUTs shall then be mounted in the test environment using sockets strategically located representing the coolest and hottest regions to verify T_J. This shall also include all other devices intended for the power test environment to duplicate the same cumulative heating effects. Those sockets used for the DUTs shall also be the same design as all others in the test environment. The DUTs shall also be electrically connected to the TSP measuring equipment that requires a set of Kelvin-sense leads to monitor junction voltage. The leads shall be attached so as to minimize heat sinking. Also see step 6.5 on further ACOL considerations.

6.3 Test environment measurement.

6.3.1 Ambient temperature. The ambient temperature (T_A) shall be as specified at thermal equilibrium conditions including any convection or circulating air effects in an oven chamber where applicable. For hot-plate applications, the surface temperature and uniformity shall also be as specified to achieve desired case temperature (T_C) control as exemplified in 6.1.1 and 6.4.1c.

6.3.2 Appling current or power. The same heating current (or equivalent rms power) shall be applied in increasing increments for all devices while sampling for TSP on each DUT with a low duty factor at I_M in accordance with equipment description in 5.4. Working with each serialized DUT one at a time, monitor the junction voltage TSP at I_M while slowly increasing the heating current. The TSP will decline with increasing T_J for V_F or V_{BE}.

6.3.3 TSP for the desired T_J. Step 6.3.1 and 6.3.2 shall be repeated until the same TSP is achieved for the desired T_J in step 6.1.2 on the sample DUTs after the same equivalent current or rms power is applied for all devices in the test environment. The power applied for this desired T_J level for each DUT shall be recorded. The average power for the DUTs shall also be determined and used as the value thereafter for applied power per unit during burn-in or life test in step 6.3.4. If thermal resistance from junction to ambient $R_{\theta JA}$ is desired for future reference as described in 10.2, the T_A should also be recorded at this time.

NOTE: The T_J is also selected based on overall tolerances of the test environment. Also see 10.3 and EQ 9 for slight T_J variations with the averaging effects of applied power above. For worst-case tolerances, the T_J should be placed nominally at the midpoint between the minimum and maximum allowed T_J required for the test environment. For example this may be 155°C if the minimum is 135°C and maximum is 175°C. If either the applied heating-power P_H or the desired T_J exceeds the DUT ratings, see steps 6.3.3.1 and 6.3.3.2. If not, proceed to 6.3.4.

6.3.3.1 Current and power ratings. If applied heating current or power P_H exceeds the rating of the device for burn-in screening to achieve the desired T_J, the following options apply:

a. The heat sinking may be reduced in the test environment.

b. The ambient temperature (T_A) may be increased until the desired T_J is achieved when allowed in the applicable performance specification.

c. The current or power may be increased not to exceed the current density capability of the device.

6.3.3.2 T_J for JANS. The T_J may be higher than typical device ratings of 150°C to 200°C when applied to JANS life test of MIL-PRF-19500 for a faster accelerated test environment. These may be specified at T_J values of 225°C to 275°C. However these options shall not exceed temperatures where the DUTs (and remaining devices) cannot operate effectively as a semiconductor in the test environment. This may also be identified as the intrinsic or secondary breakdown region (thermal generation of electron-hole pairs starts approaching or exceeding the background doping levels of the pn junctions). This may also be observed by significant increases in reverse leakage current or in more severe cases the decline (or collapse) of reverse breakdown voltage V_{BR} on rectifiers, V_Z for higher voltage zeners, or V_{CE} for transistors. Also see note in 6.4.1b for rectifiers.

6.3.4 Criteria once T_J is achieved. After the desired T_J is achieved for all devices, the burn-in or life test may proceed with the average power per unit in 6.3.3 until completed for the required number of hours.

6.4 Power requirements. It is desirable to apply the same type of rms heating power required for the test environment in 6.3 for each DUT as applied to all other devices before switching to the I_M level for measuring the TSP. However power supply equipment for thermal resistance test methods using dc forward heating current I_H and a low duty factor sample-and-hold method at I_M for the TSP may not offer that added flexibility. In such cases, the same equivalent rms heating power (P_H) may be used with a forward-heating current (I_H) as described in thermal resistance test methods where $P_H = I_H \times V_H$. When equivalent rms heating power is in question, the duplication of lead, case, or end-cap temperatures (T_L, T_C or T_{EC}) is required to verify identical rms power as described in step 6.5 for ACOL considerations.

6.4.1 Test environment and DUT power options

a. Signal and Schottky Diodes (dc burn-in with I_F): The required heating power is forward dc current (I_F) multiplied times the forward voltage (V_F) observed during the dc burn-in or life test (or $P_H = I_F \times V_F$). No equipment handicaps should exist with this test environment since I_F equates to the forward heating current I_H for thermal resistance test methods.

b. Rectifiers (ACOL burn-in with I_O): The required ac operating life at rated I_O may be approximated in equivalent rms heating power by $P_H = I_O(0.107 + 0.785\ V_{FM})$ where V_{FM} is the peak forward voltage observed during the half-sine wave and I_O is the rated average rectified output current for 50 Hz or 60 Hz sine-wave input and a 180 degree conduction angle (see JESD282-B). With this definition, the peak forward current in each half-sine wave is $3.14 \times I_O$. This P_H also assumes the power in the reverse direction is negligible due to leakage current (I_R) and applied reverse voltage (V_{RRM}) as defined in JESD282-B or method 1038 of MIL-STD-750.

   For equipment limitations to measure TSP, the DUT samples may also use the same effective forward power where P_H is the forward heating current I_H multiplied times the forward heating voltage V_H as described in 6.4. The same effective power with ACOL may be verified with identical T_L, T_C or T_{EC}. See step 6.5 to measure T_L, T_C, or T_{EC}. Also see Background information in 9.3 for the "Correlation of RMS Power with T_L, T_C or T_{EC}".

   NOTE: A reverse power loss may not be observed if "limiting resistors" have externally absorbed the intended reverse voltage (V_{RRM}) in an ACOL test environment due to high leakage currents (I_R x R voltage drop), or due to collapsing voltage as described in 6.3.3.2. The required V_{RRM} must be sample monitored to verify it has been successfully applied where applicable to all the other remaining rectifier devices under ACOL power. Limiting or ballast resistors are often used in series with each device that are then placed in parallel array connections with typical power supplies for burn-in or life test methods. This regulates I_O or limits excessive current flow if a device electrically degrades or shorts to allow continued burn-in or life testing of remaining devices for the period of time required.

c. Schottky (HTRB burn-in with I_R): To minimize high power and burn-in current levels, the required P_H is applied as an HTRB with reverse voltage (V_R) and selected range of reverse current (I_R) for all devices at elevated temperature. At low power where there is no significant self-heating, the T_C may be assumed the same value as T_J. In this example, the $P_H = I_R \times V_R$ where I_R is increased at elevated temperature. For test equipment options the DUT sample may also use the equivalent forward rms power (P_H) as described in 6.4. Where applicable, the T_C may simply be measured directly for the T_J equivalent as described in 8.

d. Zeners (dc burn-in with I_Z): The required P_H is the zener burn-in current (I_Z) multiplied times the nominal zener voltage (V_Z) where $P_H = I_Z \times V_Z$. The V_Z is also adjusted for the expected T_J using the rated temperature coefficient of the zener (α_{VZ}). For equipment limitations, the DUT sample may use the equivalent forward rms power (P_H) as described in 6.4.

e. Transistors (dc burn-in with I_C): The required heating power is the collector current (I_C) multiplied times the collector emitter voltage (V_{CE}) during the dc burn-in or life test plus any significant base current (I_B) multiplied times base-emitter voltage (V_{BE}) where $P_H = I_C \times V_{CE} + I_B \times V_{BE}$. Typically the $I_B \times V_{BE}$ power may be negligible. The low duty factor sample measurement for the TSP shall be with the same conditions as in step 6.1.2.

6.5 ACOL considerations (rectifiers). If the parts for burn-in or life test are to receive ACOL conditions, an additional step must be added after step 6.2.1 to ensure equivalent heating and T_J to the DUT samples.

6.5.1 Thermocouple mounting. When the voltage monitoring leads are being attached to the DUTs for testing in the burn-in configuration in step 6.2.1, also solder on a fine 36 AWG bare-wire thermocouple to each of them. The thermocouple should be mounted at zero distance from the body of the part. The thermocouple must be mounted to not interfere when the DUT is placed in the burn-in or life test fixtures.

6.5.2 Thermocouple usage. Also solder a thermocouple as described in 6.5.1 to the nearest device of each DUT location that receives ACOL power in the test environment.

6.5.3 Thermocouple temperature. As each of the serialized DUT parts are set to the desired junction temperature using the dc current method in the burn-in or life-test environment, also record the thermocouple temperature reading. These thermocouple readings are then used to set the ac power levels in the next step.

6.5.4 Average T_J. Apply power to heat the remaining diodes using the required ACOL while monitoring the thermocouple temperature. Increase the ac power input until the thermocouple in 6.5.2 reaches the temperature level of the DUTs in 6.5.3 at the desired junction temperature. Record the ACOL power conditions applied for each device described in 6.5.2. These values are then averaged for determining ACOL power applied for all devices. This process guarantees that all the devices will be tested at the required average junction temperature for burn-in or life test. Also see 9.3 for further background information.

NOTE: The rectifier diode with the lowest V_F and (or) the lowest ambient temperature T_A position in the test environment would require the greatest power for a given thermocouple reading to ensure the same T_J is achieved.

7. Procedure for method B. This method uses a sequential set of current pulses to characterize the TSP at the T_J in the same operating current region expected for the burn-in or life-test environment. The DUTs are a sample of devices where the TSP is recorded at the desired temperature. They shall also be of the same construction as other devices in the test environment and shall be of sufficient quantity to provide a good sample for averaging. Unless otherwise specified, this shall be a minimum of five devices.

7.1 TSP measurement. First determine the nominal T_J desired for the burn-in or life test. For military burn-in screening, the minimum T_J shall be specified by the applicable performance specification. The maximum T_J is the rating for the DUT unless otherwise specified.

7.1.1 T_J desired. In a separate temperature controlled chamber, bath, or hot plate environment, the nominal T_J desired for the burn-in or life test will initially be established within plus or minus 2°C (or as required) for recording the TSP. Additional T_J tolerance considerations are also noted in 7.3.3.

7.1.2 Recording TSP measurements. A sample-and-hold tester must be programmed for recording a sequential set of TSP measurements at operating currents in the same vicinity as anticipated for the test environment. This will perform incremental pulse V_F-I_F, V_Z-I_Z, or V_{BE}-I_{CE} tests.

a. Choose the incremental current range so that the recorded values will be centered near the current level that is expected for the burn-in or life test environment.

b Program the sample-and-hold test equipment to record junction TSP voltage readings with a sufficiently low duty factor that will not warm the DUT when taking sequential readings. Typical test parameters for a leaded-switching diode might be as follows:

(1) 0.5 ms pulse width.

(2) 1 second wait interval.

(3) 500 mA starting level for I_F.

(4) 20 steps at 5 mA increasing increments.

NOTE: The smaller the incremental steps, the more accurate the chart will be when correlating to values taken in burn-in or life test. Since this test is performed with a low duty-factor power and thermally stable parts, any holding fixture may be used, but Kelvin leads are required.

7.1.3 Data. After the DUTs have been introduced and brought to thermal equilibrium, the TSP shall be recorded in a serialized manner by cycling each part through the expected current range and printing out the data for each identified device. Each set of data is applicable only for that particular serialized part and junction temperature.

7.2 Test environment mounting

7.2.1 Verify T_J. The sample DUTs shall then be mounted in the test environment using sockets strategically located representing the coolest and hottest regions to verify T_J. All other devices intended for burn-in or life-test shall also be mounted in the test environment to duplicate the same cumulative heating effects. Those sockets used for the DUTs shall also be the same design as all others in the test environment. The DUTS shall also be electrically connected to the TSP measuring equipment that requires a set of Kelvin sense leads to monitor junction voltage. These leads shall be attached so as to minimize heat sinking. Also see step 7.4 for ACOL considerations.

7.3 Test environment measurement.

7.3.1 Thermal equilibrium. The ambient temperature (T_A) shall be as specified at thermal equilibrium conditions including any convection or circulating air effects in an oven chamber where applicable.

7.3.2 Desired level. A common heating current shall be applied in increasing increments for all devices while sampling for TSP on each DUT. Working with each serialized DUT one at a time, monitor the junction voltage TSP while slowly varying the common junction current. When the DUT being monitored is at thermal equilibrium where both its current and voltage readings match a set of readings on the chart taken in step 7.1.3, the T_J of that DUT is known to be at the desired level. This is graphically displayed on Figure 3100-1. For accuracy, the voltage readings should optimally use the same test equipment that can record in both a sample-and-hold mode in step 7.1.3 and continuously in this step.

7.3.3 Desired T_J. Paragraph 7.3.2 shall be repeated until both the current and voltage readings match a set of corresponding readings for the desired T_J level on each serialized DUT after the same equivalent rms power is applied for all devices in the test environment. The power applied for this desired T_J level for each DUT shall be recorded. The average power for the DUTs shall also be determined and used as the value thereafter for applied power per unit during burn-in or life test in 7.3.4. If the thermal resistance from junction to ambient $R_{\theta JA}$ is desired for later reference as indicated in 10.2, the T_A should also be recorded.

NOTE: The T_J is also selected based on overall tolerances of the test environment. Also see paragraph 10.3 and EQ 9 for slight T_J variations with the averaging effects of applied power above. For worst-case tolerances, the T_J should be placed nominally at the midpoint between the minimum and maximum allowed T_J required for the test environment. For example this may be 155°C if the minimum is 135°C and maximum is 175°C. If either the applied heating-power P_H or the desired T_J exceeds the DUT ratings, see 7.3.3.1 and 7.3.3.2. If not, proceed to 7.3.4.

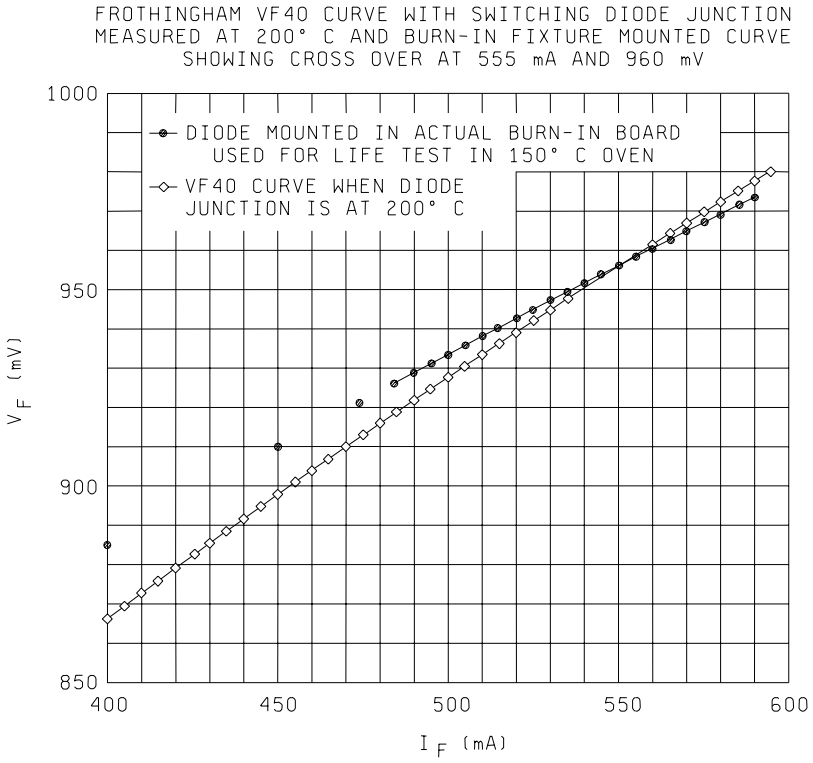


FIGURE 3100-1. Frothingham VF40 curve.

7.3.3.1 Power rating. If the applied heating power P_H exceeds the rating of the device for burn-in screening to achieve the desired T_J, the following options apply:

a. The heat sinking may be reduced in the test environment.

b. The ambient temperature T_A may be increased until the desired T_J is achieved when allowed by the applicable performance specification.

c. The current or power may be increased not to exceed the current density capability of the device.

7.3.3.2 T_J for JANS. The T_J may be higher than typical device ratings of 150°C to 200°C when applied to JANS life test in groups B, C, and E of MIL-PRF-19500 for a faster accelerated test environment. These may be specified at T_J values of 225°C to 275°C. However these options shall not exceed temperatures where the DUTs (and remaining devices) cannot operate effectively as a semiconductor in the test environment. This may also be identified as the intrinsic or secondary breakdown region (thermal generation of electron-hole pairs starts approaching or exceeding the background doping levels of the pn junctions). This may also be observed by significant increases in reverse leakage current or in more severe cases the decline (or collapse) of reverse breakdown voltage V_{BR} on rectifiers, V_Z for higher voltage zeners, or V_{CE} for transistors. Also see note in 6.4.1b for rectifiers.

7.3.4 Desired T_J After the desired T_J is achieved for all devices, the burn-in or life test may proceed with the average power per unit in 7.3.3 until completed for the required number of hours.

7.4 ACOL considerations (rectifiers). If the sample-and-hold test equipment is equipped with synchronized test capabilities for measuring the TSP voltage in the desired forward conducting half-cycle region for ACOL operation, this can again be tested in a similar manner described in 7.3. As described in 7.3.2, this should optimally be provided with the same voltage test equipment. For synchronized capabilities, a Frothingham model VF40DB or equivalent may be used. If a synchronized test capability is not available, alternative steps must be added after step 7.2.1 to ensure equivalent heating and T_J to the DUT samples. These are described in 7.4.1 through 7.4.4.

7.4.1 Thermocouple mounting. When the voltage monitoring leads are being attached to the DUTs for testing in the burn-in configuration in 7.2, also solder on a fine 36 AWG bare-wire thermocouple to each of them. The thermocouple should be mounted at zero inch distance from the body of the part. The thermocouple will have to be mounted so as to not interfere when the DUT is placed in the burn-in or life test fixtures.

7.4.2 Thermocouple usage. Also solder a thermocouple as described in 7.4.1 to the nearest device of each DUT location that receives ACOL power in the test environment.

7.4.3 Thermocouple temperature. As each of the serialized DUT parts is set to the desired junction temperature using the dc current method in the ACOL test environment, also record the thermocouple temperature reading. These thermocouple readings are then used to set the ac power levels in the next step.

7.4.4 Average T_J. Apply power to heat the remaining diodes using the required ACOL while monitoring the thermocouple temperature. Increase the ac power input until the thermocouple in 7.4.2 reaches the temperature level of the DUT in 7.4.3 at the desired junction temperature. Record the ACOL power conditions applied for each device described in 7.4.2. These values are then averaged for determining ACOL power applied for all devices. This process guarantees that all the devices will be tested at the required average junction temperature for burn-in or life test. Also see 9.3 for further background information.

NOTE: The rectifier diode with the lowest V_F and (or) the lowest ambient temperature (T_A) position in the test environment would require the greatest power for a given thermocouple reading to ensure the same T_J is achieved.

8. Procedure for method C. This method only applies to case mounted power devices where the operating power or current region expected for the burn-in or life-test environment is still well below that of the rating of the device. In these examples, the T_J of the device is not significantly higher than the case temperature T_C. This operating feature and direct measurement of case temperature may be used to confirm the minimum required T_J is met for the burn-in or life-test environment.

9. Background information.

9.1 Equations for T_J, T_A, P_H, and $R_{\theta JA}$. The observed values of the T_J rise above T_A in the test environment would be the product of effective rms heating power (P_H) multiplied times the total effects of component thermal resistance from junction to ambient ($R_{\theta JA}$).
This may also be stated as follows:

$$T_J = T_A + P_H \times R_{\theta JA} \qquad \text{EQ 1}$$

The T_A is the ambient temperature in the immediate vicinity of an open-burn-in rack or the ambient inside a convection-oven chamber for life test. If T_A is recorded at step 6.3.3 or 7.3.3, then the $R_{\theta JA}$ can also be determined as follows:

$$R_{\theta JA} = (T_J - T_A)/P_H \qquad \text{EQ 2}$$

9.2 Thermal resistance definitions for $R_{\theta JL}$, $R_{\theta JC}$, $R_{\theta JEC}$, $R_{\theta LA}$, $R_{\theta CA}$, and $R_{\theta ECA}$. The thermal resistance $R_{\theta JA}$ is the total of the DUT thermal resistance junction to lead or case ($R_{\theta JL}$ or $R_{\theta JC}$), and the thermal resistance of the test environment from lead or case (test socket) to ambient ($R_{\theta LA}$ or $R_{\theta CA}$). For example:

$$R_{\theta JA} = R_{\theta JL} + R_{\theta LA}$$
or
$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

This also applies to surface mount devices that may use an end cap (EC) reference rather than case. In this example:

$$R_{\theta JA} = R_{\theta JEC} + R_{\theta ECA}$$

The T_J in each of these examples can be determined as follows:

$$T_J = T_A + P_H \times (R_{\theta JL} + R_{\theta LA}) = T_L + P_H \times R_{\theta JL} \qquad \text{EQ 3}$$
$$T_J = T_A + P_H \times (R_{\theta JC} + R_{\theta CA}) = T_C + P_H \times R_{\theta JC} \qquad \text{EQ 4}$$
$$T_J = T_A + P_H \times (R_{\theta JEC} + R_{\theta ECA}) = T_{EC} + P_H \times R_{\theta JEC} \qquad \text{EQ 5}$$

Earlier methods have also determined T_J based on these relations that use thermal resistance of the component and also the reference point temperature (T_L, T_C, T_{EC}) measured in the test environment with applied power P_H. Possible sources of error included the use of maximum rated thermal resistance rather than actual value (see note), nonlinear features affecting thermal resistance or K factor at notably higher temperatures during life test, and difficulty in measuring reference temperature (T_L, T_C, T_{EC}) particularly for enclosed convection air ovens.

NOTE: For accurate determination of T_J, this requires the actual component thermal resistance value rather than the maximum rating. This distinction is important to ensure adequate T_J values are achieved in 6.3.3 or 7.3.3.

9.3 Correlation of RMS power with T_L, T_C, or T_{EC}. The lead, case, or end-cap temperature reference points within the test environment are as follows:

$$T_L = T_A + P_H \times R_{\theta LA} \qquad \text{EQ 6}$$
$$T_C = T_A + P_H \times R_{\theta CA} \qquad \text{EQ 7}$$
$$T_{EC} = T_A + P_H \times R_{\theta ECA} \qquad \text{EQ 8}$$

If the T_L, T_C or T_{EC} is the same between any two devices in identical test environment conditions for ambient temperature and thermal resistance of the test socket from component to ambient, then the effective rms power must be the same between them as may be observed in EQ 6, 7, and 8. This feature may be used to advantage in determining equivalent heating power levels in different power modes as described in 6.5 and 7.4. Also when the same equivalent heating power levels are applied to devices of identical design with the same thermal resistance at the same T_L, T_C or T_{EC}, then the same T_J is achieved as shown in EQ 3, 4, and 5.

10. Summary.

10.1 Repeatable T_J values. This procedure may not require repeating for every lot processed for burn-in and life-test if this method verifies the same T_J values (within acceptable tolerances) for thermally identical test environments and devices to be tested as demonstrated in 9.1 and EQ 1. This would occur in a test environment with the same T_A and heat-sinking effects ($R_{\theta LA}$, $R_{\theta CA}$, or $R_{\theta ECA}$), as well as components of the same thermal resistance ($R_{\theta JL}$, $R_{\theta JC}$, or $R_{\theta JEC}$). These conditions provide the same effective $R_{\theta JA}$ and the same T_J values as demonstrated in 9.2. The value of $R_{\theta JA}$ is determined by the following in 10.2.

10.2 The effective thermal resistance. $R_{\theta JA}$ for the test environment can be determined for the devices or DUTs with the heating power P_H recorded at 6.3.3 or 7.3.3 with ambient temperature (T_A) and junction temperature (T_J) with EQ 2 in 9.1. The $R_{\theta JA}$ for identical test environments and products can then be used to advantage for determining other desired T_J values when needed at applied power levels P_H or ambient temperature (T_A) conditions.

10.3 Average power. When an individual (average) power level P_H is selected for the test environment in 6.3.3 or 7.3.3, small variations in power ΔP_H to this average will exist over the sample number of DUTs to achieve the same TSP or T_J. As a result, slight variations in ΔT_J will also occur for continuing the burn-in or life test in 6.3.4 or 7.3.4 with typical power supplies and wiring harnesses. This ΔT_J may also be determined from EQ 1 as shown below in EQ 9.

$$\Delta T_J = T_A + \Delta P_H \times R_{\theta JA} \qquad \text{EQ 9}$$

This added consideration for T_J tolerances in 6.3.3 or 7.3.3 is of interest since the same operating current or power condition is applied to all devices for continuing burn-in or life test in 6.3.4 or 7.3.4 with typical power supplies and wiring harnesses. These slight T_J variations may be from small variations in socket and component thermal resistance. It may also be from notable variations in ambient temperature in the immediate vicinity of each DUT placed at different locations in the test environment.

METHOD 3131.4

*STEADY-STATE THERMAL IMPEDANCE AND TRANSIENT THERMAL IMPEDANCE TESTING OF TRANSISTORS (DELTA BASE – EMITTER VOLTAGE METHOD)

* 1. Purpose. The purpose of this test is to determine the thermal performance of transistor devices. This can be done in two ways, steady-state thermal impedance or thermal transient testing. Steady-state thermal impedance (referred to as thermal resistance) determines the overall thermal performance of devices. A production-oriented screening process, referred to as transient thermal impedance testing, is a subset of steady-state thermal impedance testing and determines the ability of the transistor chip-to-header interface to transfer heat from the chip to the header, and is a measure of the thermal quality of the die attachment. It is relevant to designs which use headers, or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor die attachments. This is particularly true with power devices. The method can be applied to small signal, power, switching and Darlington transistors. This method is intended for production monitoring, incoming inspection, and pre-burn in screening applications. The measurement current (IM) must be large enough to ensure that the Darlington output transistor is biased into the linear conduction mode of the temperature sensing measurement periods of the thermal test.

* 1.1 Background and scope for transient thermal impedance testing. Transient thermal impedance of semiconductor devices are sensitive to the presence of voids in the die attachment material between the semiconductor chip and package since voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal impedance can be made more sensitive to the presence of voids than can the measurement of steady-state thermal impedance. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the substrate. Heating power pulse widths ranging from 1 to 400 ms for various package designs have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heat sink the device under test (DUT). Thus, the transient thermal impedance techniques are less time consuming than the measurement of thermal resistance for use as a manufacturing screen, process control, or incoming inspection measure for die attachment integrity evaluation.

* 2. Definitions. The following symbols and terminology shall apply for the purpose of this test method:

a. V_{BE}: The forward biased base-emitter junction voltage of the DUT used for junction temperature sensing.

V_{BEi}: The initial V_{BE} value during application of measurement current (IM) and before application of heating power.

V_{BEf}: The final V_{BE} value during the sample window time (t_{SW}) after application and subsequent removal of heating power.

b. ΔV_{BE}: The change in, V_{BE}, (VBEi-VBEf) due to the application of heating power to the DUT.

c. I_H: The collector current applied to the DUT during the heating period.

d. V_{CE}: The voltage between the collector and emitter. V_{CE} is constant throughout the test.

e. P_H: The heating power applied the DFUT. $P_H = I_H . x\ V_{CE}$.

f. t_H: The duration of the heating power pulse P_H.

g. ti: The time after application of the measurement current (IM) and before application of the heating power pulse.

h. I_M: The measurement current applied to forward bias the junction for measurement of V_{BE}.

i. t_{MD}: Measurement delay time is the time from the end of the heating power pulse to the beginning of the sample window time (t_{SW}). Delay must be sufficient in length to allow for attenuation of switching transients to occur. The delay time will vary according to the length of the cable to test fixture and associated fixture inductances.

j. t_{SW}: Sample window time during which final V_{BE} measurement is made. The value of t_{SW} should be small; and occur at precisely the conclusion of tMD. It can approach zero if an oscilloscope is used for manual measurements and no transient effects are present.

k. VTC: Voltage-temperature coefficient of V_{BE} with respect to T_J at a fixed value of I_M; in mV/°C.

l. K: Thermal calibration factor equal to the reciprocal of VTC; in °C/mV.

* m. CU: The comparison unit, consisting of ΔV_{BE} divided by V_{BE}, that is used to normalize the transient thermal impedance for variations in power dissipation; in units of mV/V.

n. T_J: The DUT junction temperature.

o. ΔT_J: The change in T_J caused by the application of P_H for a time equal to t_H.

* p. $Z_{\theta JX}$: Transient. Thermal impedance from device junction to a time defined reference point; in units of °C/W.

* q. $Z_{\theta JC}$: Transient. Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device chip measured using time equal time constant of device; in units of °C/W.

* r. $R_{\theta JX}$: Steady-state. Thermal resistance from device junction to a defined reference point; in units of °C/W.

* s. $R_{\theta JC}$: Steady-state. Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip; in units of °C/W.

* t. $R_{\theta JA}$: Steady-state. Thermal resistance from device junction to an ambient (world); in units of °C/W.

u. TSP: The temperature sensitive parameter; V_{BE}.

3. Apparatus. The apparatus required for this test shall include the following, configured as shown on figure 3131-1, as applicable to the specified test procedure:

a. A constant current source capable of adjustment to the desired value of I_H and able to supply the V_{BE} value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire length of heating time.

b. A constant current source to supply I_M with sufficient voltage compliance to turn the TSP junction fully on.

c. An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.

d. A voltage measurement circuit capable of accurately making the V_{BEf} measurement within the time frame with millivolt resolution.

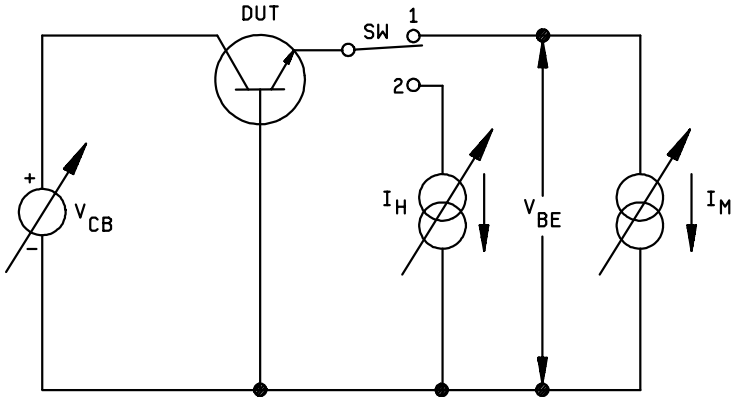


FIGURE 3131-1. Thermal impedance testing setup for transistors.

4. Test operation.

4.1 General description. The test begins with the adjustment of I_M and I_H to the desired values. The value of I_H is usually at least 50 times greater than the value of I_M. Then with the electronic switch in position 1, the value of V_{BEi} is measured. The switch is then moved to position 2 for a length of time equal to t_H and the value of V_{BE} is measured. Finally, at the conclusion of t_H, the switch is again moved to position 1 and the V_{BEf} value is measured within a time period defined by t_{MD} (or $t_{MD} + t_{SW}$, depending on the definitions stated previously). The two current sources are then turned off at the completion of the test.

4.2 Notes.

a. Some test equipment may provide a ΔVBE directly instead of V_{BEi} and V_{BEf}; this is an acceptable alternative. Record the value of ΔV_{BE}.

b. Some test equipment may provide $Z_{\theta JX}$ directly instead of V_{BEi} and V_{BEf} for thermal resistance calculations; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.

c. Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used upon approval of the qualifying activity.

5. Acceptance limit.

5.1 General discussion. Variations in transistor characteristics from one manufacturer to another cause difficulty in establishing a single acceptance limit for all transistors tested to a given specification. Ideally, a single acceptance limit value for ΔV_{BE} would be the simplest approach. However, different design, materials, and processes can alter the resultant ΔV_{BE} value for a given set of test conditions. Listed below are several different approaches to defining acceptance limits. The ΔV_{BE} limit is the simplest approach and is usually selected for screening purposes. Paragraphs 5.3 through 5.6 require increasingly greater detail or effort.

5.2 ΔV_{BE} limit. A single ΔV_{BE} limit is practical if the K factor and V_{BE} values for all transistors tested to a given specification are nearly identical. Since these values may be different for different manufacturers, the use of different limits is likely to more accurately achieve the desired intent. (A lower limit does not indicate a better die bond when comparing different product sources.) The transistor specifications would list the following test conditions and measurement parameters:

a. I_H (in A).

b. t_H (in ms).

c. I_M (in mA).

d. t_{MD} (in µs).

e. t_{SW} (in µs).

f. ΔV_{BE} (maximum limit value, in mV).

5.3 ΔT_J limit. (Much more involved than ΔVBE , but useful for examining questionable devices.) Since ΔT_J is the product of K (in accordance with 6.) and ΔV_{BE}, this approach is the same as defining a maximum acceptable junction temperature rise for a given set of test conditions.

5.4 CU limit. (Slightly more involved than ΔT_J.) The ΔT_J limit approach described above does not take into account potential power dissipation variations between devices. The V_{BE} value can vary, depending on chip design and size, thus causing the power dissipation during the heating time to be different from device to device. This variation will be small within a lot of devices produced by a single manufacturer but may be large between manufacturers. A CU limit value takes into account variations in power dissipation due to differences in V_{BE} by dividing the ΔV_{BE} value by V_{BE}.

5.5 (K•CU) limit. (Slightly more involved but provides greater detail.) This is a combinational approach that takes into account both K factor and power dissipation variations between devices.

* 5.6 $Z_{\theta JX}$ limit. (For full characterization; not required for screening purposes, but preferred if the proper ATE is available.) The transient thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other approaches. transient Thermal impedance is time dependent and is calculated as follows:

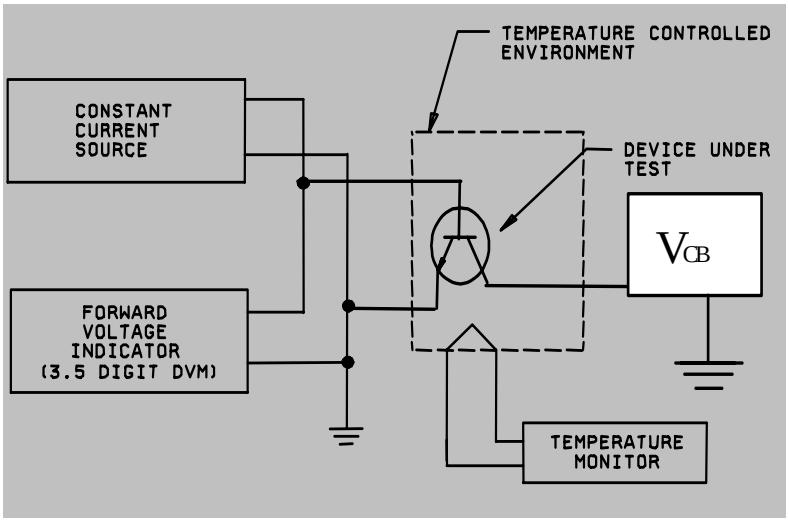
$$Z_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_{BE})}{(I_H)(V_H)} \right| {}^{o}C/W$$

5.7 $R_{\theta JX}$ limit. (For thermal resistance specification testing.) The thermal resistance to some defined point, such as the case, is an absolute magnitude value specification used for equilibrium conditions. The t_H heating time must therefore be extended to appreciably longer times (typically 20 to 50 seconds). In the example of $R_{\theta JC}$ measurements, the case must be carefully stabilized and monitored in temperature which requires an infinite heat sink for optimum results. The ΔT_J is the difference in junction temperature to the case temperature for the example of $R_{\theta JC}$.

$$R_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_{BE})}{(I_H)(V_H)} \right| {}^{o}C/W$$

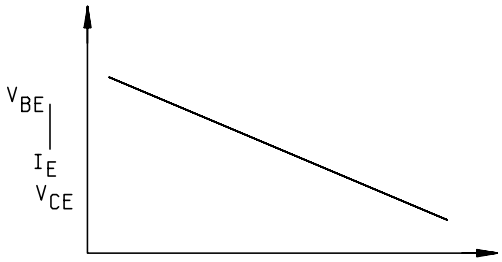
* 5.8 General comment for transient thermal impedance testing. One potential problem in using the transient thermal impedance-testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and nonacceptable transistors. As the DUT current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher I_H values must be used in this case.

6. Measurement of the TSP V_{BE}. The calibration of V_{BE} versus T_J is accomplished by monitoring V_{BE} for the required value of I_M as the environmental temperature (and thus the DUT temperature), and is varied by external heating. It is not required if the acceptance limit is ΔV_{BE} (see 5.2), but is relevant to the other acceptance criteria (see 5.3 through 5.6). The magnitude of I_M shall be chosen so that V_{BE} is a linearly decreasing function over the normal T_J range of the device. I_M must be large enough to ensure that the base-emitter junction is turned on but not large enough to cause significant self-heating. An example of the measurement method and resulting calibration curve is shown on figure 3131-2.



Step 1: Measure V_{BE1} at T_{J1} using I_M
Step 2: Measure V_{BE2} at T_{J2} using I_M

Step 3: $K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| °C/mV$



I_M: Must be large enough to overcome surface leakage effects but small enough not to cause significant self-heating.

T_J: Is externally applied (e.g., via oven, liquid) environment.

FIGURE 3131-2. Example curve of V_{BE} versus T_J.

A calibration factor K (which is the reciprocal of the slope of the curve on figure 3131-2) can be defined as:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| \ ^{\circ}C/mV$$

The K factor is used to calibrate the DUT such that the measured forward voltage drop corresponds to the temperature of the junction at a given bias condition. In order to ensure accurate results, the bias conditions used to determine the K factor must be chosen such that the application is duplicated. Therefore, the results will be unique for each particular biasing condition and should be reestablished for different values of base and/or collector currents (IF for diodes). This method should be used for each of the following conditions: Transient thermal impedance, burn-in, and life tests. Verify actual TJ seen by a device in field applications.

It has been found experimentally that the K-factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 piece to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than three percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in determining device acceptance. As an alternative to using individual values of K, the manufacture may establish internal limits unique to their product that ensures atypical product removal from the population (lot-to-lot and within-the-lot). The manufacturer shall use statistic techniques to establish the limits to the satisfaction of the government.

7. Establishment of test conditions and acceptance limits. Thermal resistance measurements require that I_H be equal to the required value stated in the device specifications, typically at rated current or higher. Values for t_H, t_{MD}, and heat sink conditions are also taken from the device specifications. The steps shown below are primarily for transient thermal impedance testing and thermal characterization purposes.

The following steps describe how to set up the test conditions and determine the acceptance limits for implementing the transient thermal test for die attachment evaluation using the apparatus and definitions stated above.

7.1 Initial device testing procedure. The following steps describe in detail how to set up the apparatus described previously for proper testing of various transistors. Since this procedure thermally characterizes the transistor out to a point in heating time required to ensure heat propagation into the case (i.e., the $R_{\theta JX}$ condition), an appropriate heat sink should be used or the case temperature should be monitored.

* Step 1: From a 20 to 25 piece sample, pick any one diode to start the setup process. Set up the test apparatus as follows:

	I_H = 1.0 A	(Or some other desired value near the DUTs normal operating current, typically higher for power transistors.
	t_H = 10-50 ms	Unless otherwise specified, for most devices rated up to 15 W power dissipation.
	50 - 100 ms	Unless otherwise specified, for most devices rated up to 200 W power dissipation.
*	≥ 250 ms	For steady-state thermal impedance measurement. The pulse must be shown to correlate to steady-state conditions before it can be substituted for steady-state condition.

t_{MD} = 100 µs max — A larger value may be required on power devices with inductive package elements which generate nonthermal electrical transients; unless otherwise specified, this would be observed in the t_3 region of figure 3131-3.

I_M = 10 mA — (Or some nominal value approximately two percent, or less, of I_H.)

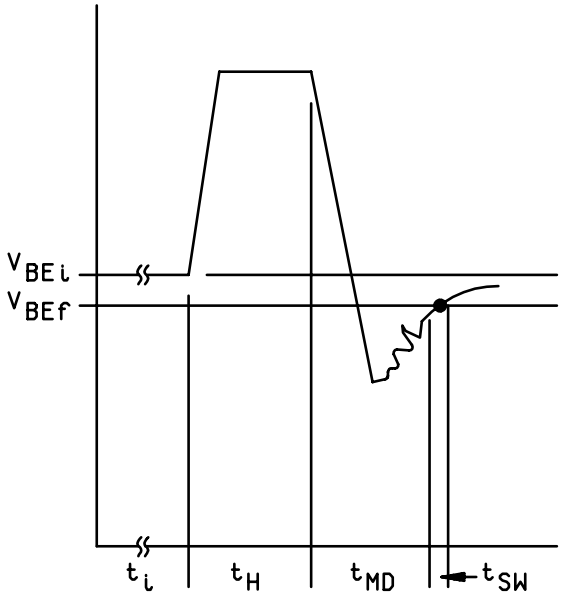


FIGURE 3131-3. Thermal impedance testing waveforms.

Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the diode's free-air rating or the maximum heating time is limited to less than that required for the heat to propagate through the case.)

Step 3: If ΔV_{BE} is in the 15 to 80 mV range then proceed to the next step. This range approximately corresponds to a junction temperature change of roughly +10°C to +50°C and is sufficient for initial comparison purposes.

If ΔV_{BE} is less than 15 mV, return to 7.1, step 1 and increase heating power into device by increasing I_H.

If ΔV_{BE} is greater than 80 mV, approximately corresponding to a junction temperature change greater than +50°C, it would be desirable to reduce the heating power by returning to 7.1, step 1 and reducing I_H.

NOTE: The test equipment shall be capable of resolving ΔV_{BE} to within five percent. If not, the higher value of ΔV_{BE} must be selected until the five percent tolerance is met. Two different devices can have the same junction temperature rise even when P_H is different, due to widely differing V_{BE}. Within a given lot, however, a higher V_{BE} is more likely to result in a higher junction temperature rise. For such examples, this screen can be more accurately accomplished using the CU value. As defined in 2m., CU provides a comparison unit that takes into account different device V_{BE} values for a given I_H test condition.

Step 4: Test each of the sample devices and record the data detailed in 8.1.

Step 5: Select out the devices with the highest and lowest values of CU or $Z_{\theta JX}$ and put the remaining devices aside.

The ΔV_{BE} values can be used instead of CU or $Z_{\theta JX}$ if the measured values of V_{BE} are very tightly grouped around the average value.

Step 6: Using the devices from 7.1, step 5, collect and plot the heating curve data for the two devices in a manner similar to the examples shown on figure 3131-4.

Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the heating time (t_H) is less than or equal to the thermal time constant of the chip, the two curves should start out the same for the low values of t_H. Non-identical chips (thinner or smaller in cross section) will have completely different curves, even at the smaller values of t_H. As the value of t_H is increased, thereby exceeding the chip thermal constant, heat will have propagated through the chip into the die attachment region. Since the heating curve devices of 7.1, step 5 were specifically chosen for their difference, the curves of figure 3131-4 diverge after t_H reaches a value where the die attachment variance has an affect on the device junction temperature. Increasing t_H further will probably result in a flattening of the curve as the heating propagates in the device package. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

Step 8: Using the heating curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path: Chip, die attachment, substrate, substrate attach, and package, for example in a hybrid, there will be several plateaus and transitions in the heating curve. Appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set t_H equal to the value determined from 7.1, step 8.

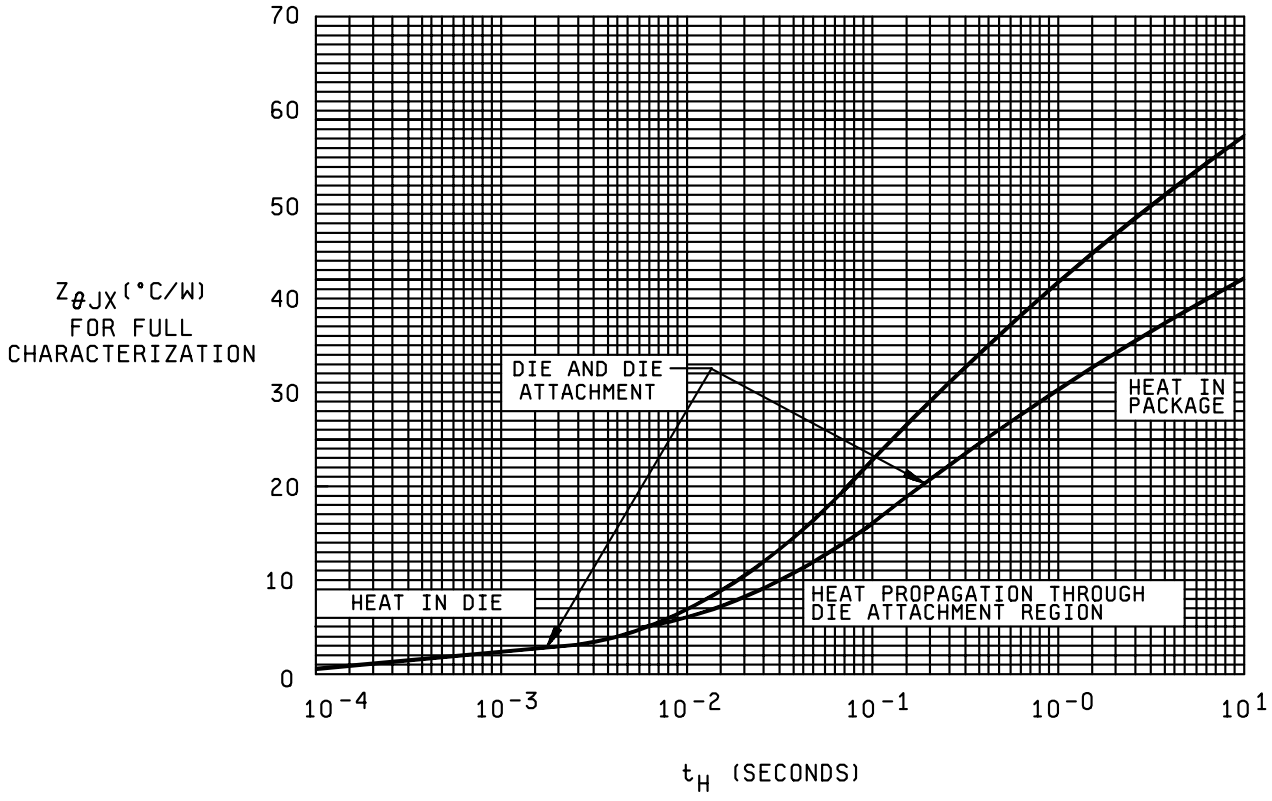


FIGURE 3131-4. Heating curves for two extreme devices.

Step 10: Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the heating power without degrading or destroying the device. The increased power dissipation within the DUT will result in higher ΔV_{BE} or CU values that will make determination of acceptable and nonacceptable devices much easier.

Step 11: The pass/fail limit, the cut-off point between acceptable and nonacceptable devices, can be established in a variety of ways:

a. Correlation to other die attachment evaluation methods, such as die shear and x-ray, while these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in various military standards.

b. Maximum allowable junction temperature variations between devices, since the relationship between ΔT_J and ΔV_{BE} is about 0.5°C/mV for forward bias testing, or 0.25C/mV for Darlington transistors, the junction temperature spread between devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections can be translated to a ΔV_{BE} or CU value for pass/fail criteria.

To fully utilize this approach, it will be necessary to calibrate the devices for the exact value of the T_J to V_{BE} characteristic. The characteristic's slope, commonly referred to as K factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature indicator, and a power supply setup as described in 6. A simple set of equations yield the junction temperature once K and ΔV_{BE} are known:

$$\Delta T_J = (K)\ (\Delta VBE)$$

$$T_J = T_A + \Delta T_J$$

Where: T_A is the ambient or reference temperature. For thermal transient test conditions, this temperature is usually equivalent to case temperature (T_C) for case mounted devices.

c. Statistically from a 20 to 25 device sample, the distribution of ΔV_{BE} or CU values should be a normal one with defective devices out of the normal range. Figure 3131-5 shows a ΔV_{BE} distribution for a sample lot of transistors. NOTE: The left-hand side of the histogram envelope is fairly well defined but the other side is greatly skewed to the right. This comes about because the left-hand side is constrained by the absolutely best heat flow that can be obtained with a given chip assembly material and process unless a test method error is introduced. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.

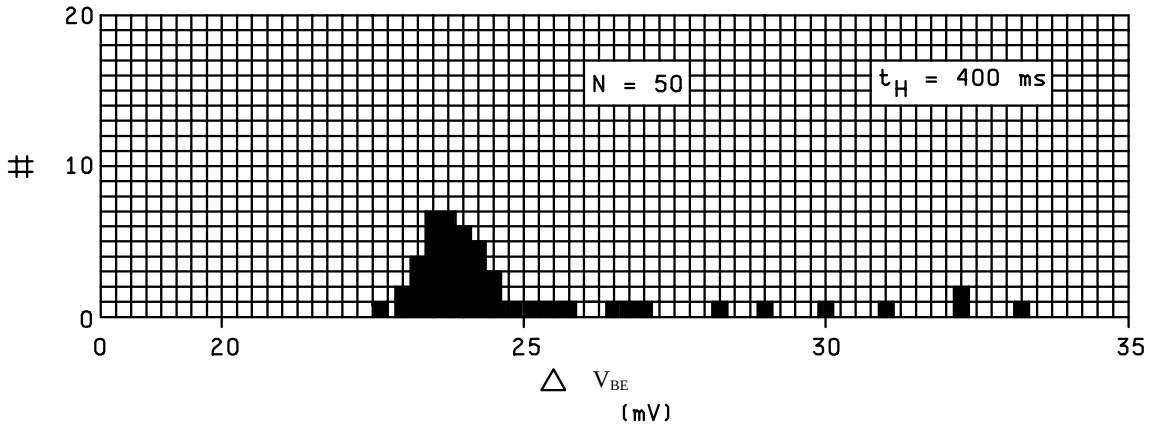


FIGURE 3131-5. Typical ΔV_{BE} distribution.

The usual rule of thumb in setting the maximum limit for ΔV_{BE} , CU, or $Z_{\theta JX}$ is to use the distribution average value and three standard deviations (σ). For example:

$$| (\Delta V_{BE}) | = \overline{\Delta V}_{BE} + X \sigma$$

high
limit

$$| (CU) | = \overline{CU} + X \sigma$$

high
limit

$$| (Z_{\theta JX}) | = \overline{Z}_{\theta JX} + X \sigma$$

high
limit

Where: X = 3 in most cases and $\overline{\Delta V}_{BE}$, $\overline{\Delta CU}$, and $\overline{\Delta Z}_{\theta JX}$ are the average distribution values.

The statistical data required is obtained by testing 25 or more devices under the conditions of 7.1, step 11.

The maximum limit determined from this approach should be correlated to the transistor's specified thermal resistance. This will ensure that the ΔV_{BE} or CU limits do not pass diodes that would fail the thermal resistance or transient thermal impedance requirements.

Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package. It is also recommended that a minimum limit is established to ensure a test method error or other anomaly is investigated.

Step 13: After the pass/fail limits are established, there shall be verification they correllate to good and bad bonded devices or the electrical properties such as surge.

The steps listed hereto are conveniently summarized in table 3131-I.

TABLE 3131-I. Summary of test procedure steps.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in 10 to 15 piece sample.
B	Heating curve generation	5 through 6	Using highest and lowest reading devices, generate heating curves.
C	Heating curve interpretation	7 through 9	Heating curve is used to find more appropriate value for t_H corresponding to heat in the die attachment area (for some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during t_H is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available such as JESD 34 for setting the fail limit; the statistical approach is the fastest and easiest to implement.
F	Verification	13	Mechanical / Electrical correlation

7.2 Routine device thermal transient testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same test conditions be used as previously determined. New device types or the same devices manufactured with a different process will require a repeat of 7.1 for proper thermal transient test conditions.

8. Test conditions and measurements to be specified and recorded.

* 8.1 Transient thermal impedance-steady-state thermal impedance measurements.

8.1.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___ mA

b. I_H heating current ___ A

c. t_H heating time ___ ms

d. t_{MD} measurement time delay ___µs

e. t_{SW} sample window time ___ µs

8.1.2 Data. Record the following data:

a. V_{BEi} initial forward voltage ___V

b. V_H heating voltage ___V

c. V_{BEf} final forward voltage ___V

(NOTE: Some test equipment may provide a ΔV_{BE} instead of V_{BEi} and V_{BEf}; this is an acceptable alternative. Record the value of ΔV_{BE}.

Some test equipment may provide direct display of calculated CU or $Z_{\theta JX}$; this is an acceptable alternative. Record the value of CU or $Z_{\theta JX}$.

8.2 K factor calibration. (Optional for criteria 8.3a or 8.3b, mandatory for 8.3c, 8.3d, or 8.3e.)

8.3 Test conditions. Specify the following test conditions:

a. I_M current magnitude ___mA

b. Initial junction temperature ___°C

c. Initial V_{BE} voltage ___mV

d. Final junction temperature ___°C

e. Final V_{BE} voltage ___mV

8.4 K factor. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| \ ^\circ C/mV$$

K factor ___°C/mV

8.5 Specification limit calculations. One or more of the following should be measured or calculated, as called for on the device specification (see 5.1):

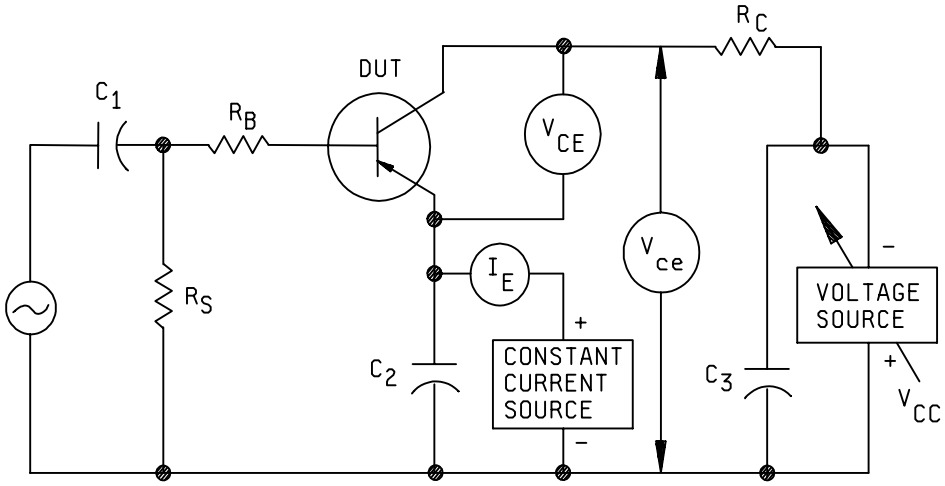
ΔV_{BE}	___mV
CU	___mV/V
ΔT_J	___°C
K•CU	___°C/V
$Z_{\theta JX}$	___°C/W
$R_{\theta JX}$	___°C/W

METHOD 3306.4

SMALL-SIGNAL SHORT-CIRCUIT FORWARD-CURRENT TRANSFER RATIO

1. Purpose. The purpose of this test is to measure the forward-current transfer ratio under the specified conditions.

2. Test circuit. The circuit (see figure 3306-1) and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly.



* NOTE: The biasing circuit shown is for purpose of illustration only. Other stable biasing circuits may be used.

FIGURE 3306-1. Test circuit for small-signal short-circuit forward-current transfer ratio.

* 3. Procedure. Capacitors C_1, C_2, and C_3 shall present short circuits in order to effectively couple and bypass the test signal at the frequency of measurement. The value of R_B shall be sufficiently large to provide a constant current source. Resistor R_C shall be a short circuit compared to the output impedance of the device. With the device removed from the circuit, a shorting link is placed between the base and collector and the output voltage of the signal generator is adjusted until a reading of one (in arbitrary units) is obtained on the high-impedance ac voltmeter, V_{ce}. With the device in the circuit and biased as specified, the reading on voltmeter V_{CE} is now equal to the magnitude of (h_{fe}). (NOTE: Care must be taken to assure that the output signal is not clipped.)

* 4. Summary. The following conditions shall be specified in the performance specification:

a. Measurement frequency.

b. Test voltages and currents.

c. Parameter to be measured.

METHOD 4023.1

SCOPE DISPLAY

1. Purpose. The purpose of this test is to define criteria for inspection of the dynamic reverse characteristics of rectifiers, switching, and zener diodes when viewed on a curve tracer. This inspection criteria may not be applicable to specific rectifier designs where the device is not intended to be driven into avalanche breakdown, or where the detail specification has not provided for this inspection.

2. Scope.

a. All devices requiring stable or sharp and stable breakdown characteristics. NOTE: Since low voltage zeners do not inherently have, and some other devices may not have a "sharp" breakdown, specific exceptions in requirements are also provided herein.

b. For condition A, stable (only) types, figures 4023-4 through 4023-11 shall apply.

c. For condition B, sharp and stable types, figures 4023-2 through 4023-11 shall apply. The ideal sharp and stable trace is one which exhibits a single horizontal line up to the point of breakdown, then transitions vertically to form a 90 degree angle while maintaining the single line (see figure 4023-1). Deviations from this ideal, which are not specifically allowed in this method or detail, specification shall be cause for rejection of the DUT. The following depictions (figures 4023-2 through 4023-11) have been compiled to describe commonly observed faults. Tolerances from acceptable devices have been assigned when applicable.

3. Procedures

a. The curve tracer presentation shall be configured so that the horizontal axis shall be calibrated in volts per division and the vertical axis shall be calibrated in amperes per division (or fractions thereof). The vertical and horizontal axis of the curve tracer presentation will be graduated into 8 or 10 divisions, each representing a precalibrated increment of current or voltage.

b. A series load resistor shall be used to limit the device reverse current and prevent device damage. This typical resistance should be approximately one quarter or more of the device resistance at the breakdown specification, when the curve trace set-up permits. Example: A device to be observed at I_{BR} of 100 μA which is specified to be 400 volts minimum, would have a series resistance chosen according to the following:

$R \geq 0.25\ (400 / 0.0001)$, therefore
$R \geq 1\ M\Omega$

The curve tracer peak voltage (V_{CT}) may also require limitation, particularly if the series load resistance described cannot be achieved. See figure 4023-1 and e. below for typical load line relationships to assure safe reverse current monitoring.

* Unless otherwise specified the breakdown current shall be the current used for the breakdown voltage test.

c. The trace should occur in the first and third quadrant of the display and be slowly adjusted from zero volts to attain the specified current with the maximum amount of resolution for determination of trace characteristics. The DUT shall be held under breakdown conditions for at least one second to ensure freedom from intermittent instability for breakdown drift. NOTE: All figures herein are shown in the first quadrant.

d. The vertical and horizontal sensitivity shall be adjusted on the curve tracer to provide a rendition of the complete trace to the specified current. Horizontal and vertical sensitivity shall be adjusted to provide a trace occupying no less than 50 percent of the available screen.

e. The curve trace voltage shall not be simply set at a predetermined value and snapped on instantaneously. This may be done only if the product to be tested is known to have a sufficiently narrow breakdown voltage (V_{BR}) range with a predetermined series (load line) resistor setting (see 3.b.) and described below, to assure that the device will not be overpowered. This is typically the case for zener diodes prescreened on V_Z (or V_{BR}). The peak open circuit supply voltage of the curve tracer (V_{CT}) may then be adjusted such that the V_{CT} setting can provide no more current (I_{BR} or I_Z) than that required for avalanche breakdown, taking into account the series load resistance "R" in figure 4023-1. Unless otherwise specified, these relationships may be calculated by:

$$I_{BR} = \frac{V_{CT} - V_{BR}}{R}, \text{ and } V_{CT} = I_{BR}R + V_{BR}$$

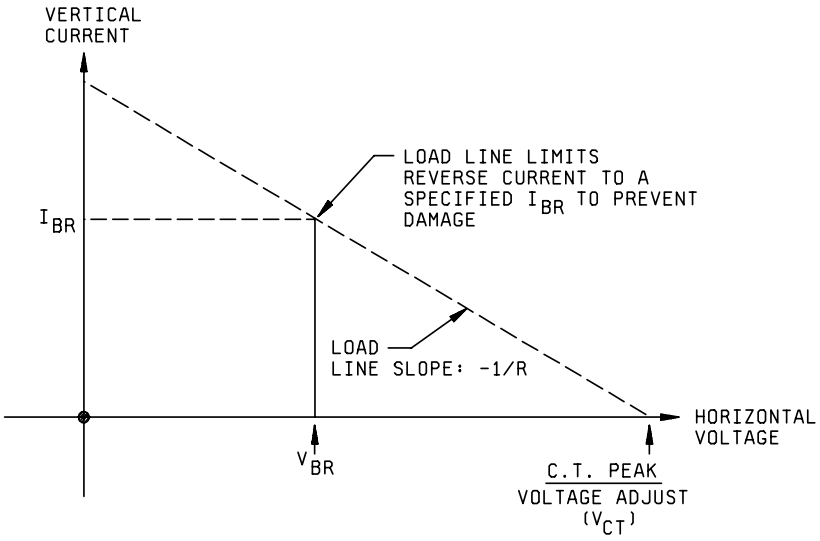
The resistance "R" may be determined by:

$$R = \frac{V_{CT} - V_{BR}}{I_{BR}}$$

The V_{BR} (or V_Z) utilized in this equation should be the minimum expected so as to always maximize the R value selected.

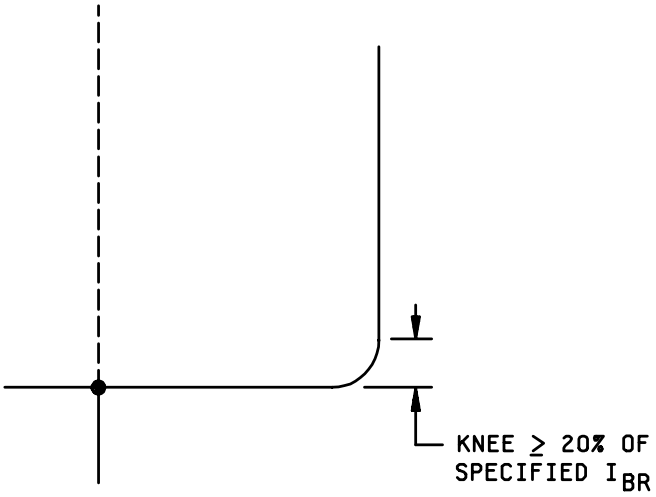
f. Allowance for deviation from the desired characteristics described in this method or detail specification must be granted by the qualifying activity. If a particular rejectable trace described is expected in a manufacturer's normal process, it must be identified and explained during device conformance/ qualification. Devices exhibiting the exceptional trace characteristic must be present in the conformance/qualification lot to establish reliability.

4. Summary. The following condition shall be specified in the detail specification: Test condition to be used.



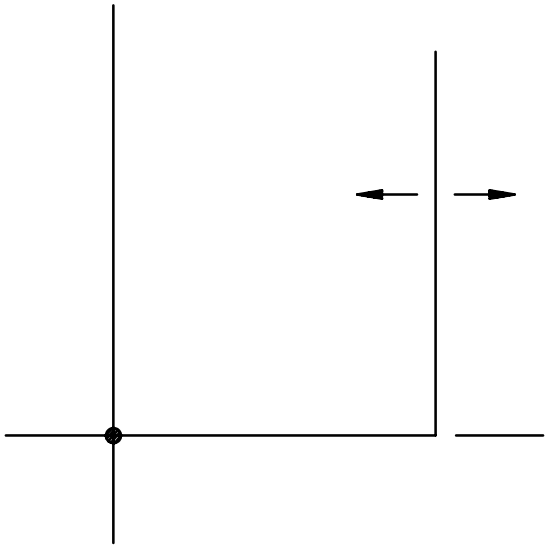
This ideal trace exhibits none of the characteristics described on the figures below. Also, illustrated are the basic curve tracer adjustments and relation for a safe maximum operating current (I_{BR}) with the series load resistor (R) versus peak open circuit voltage (V_{CT}) and device breakdown voltage (V_{BR}).

FIGURE 4023-1. Ideal reverse.



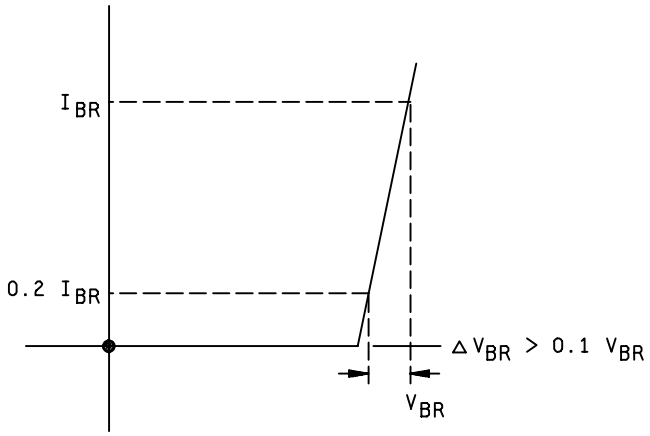
The knee area is the area in which the trace transitions from the horizontal to the vertical. Unless otherwise specified, this area should not require more than 10 percent of the total horizontal voltage component being viewed, or more than 20 percent of the specified I_{BR}. Not applicable to fast, ultrafast, and schottky rectifiers or low voltage zeners ≤ 10 volts.

FIGURE 4023-2. Soft knee.



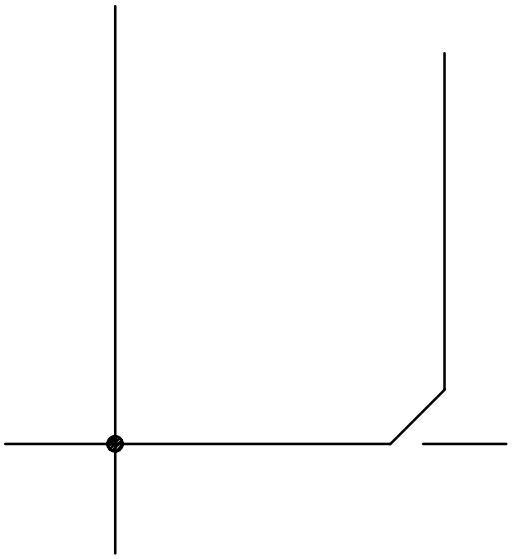
The vertical component of the trace should remain stable in the horizontal axis. An undesirable drift is defined as greater than a 10 percent increase or 2 percent decrease in actual breakdown voltage up to 1,500 volts. If over 1,500 volts, the allowable drift should be separately specified.

FIGURE 4023-3. Drift.



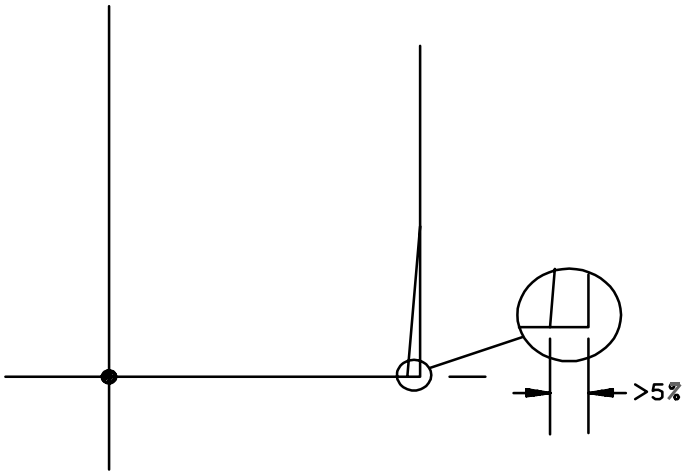
The slope shall be less than 10 percent of V_{BR} when viewed between 20 percent to 100 percent of the specified I_{BR} or I_Z. Low voltage zeners below 5.5 volts are in exception to this requirement; also or other devices, as may be specified.

FIGURE 4023-4. Slope.



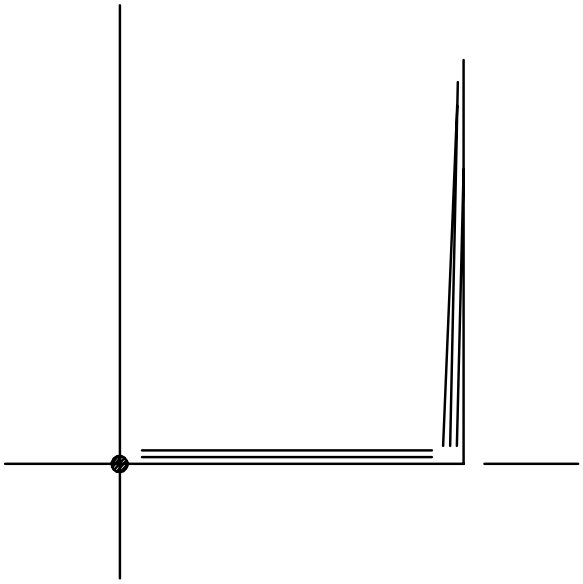
The double break is the area in which the trace transitions from the horizontal to the vertical. Unless otherwise specified, this area should not occupy more than 10 percent of the total horizontal voltage component being viewed, or more than 20 percent of the specified I_{BR} or I_{ZT}. This requirement is not applicable to ultrafast or schottky rectifiers, and low voltage zeners ≤ 10 volts.

FIGURE 4023-5. Double break (reject criteria for sharp knee devices).



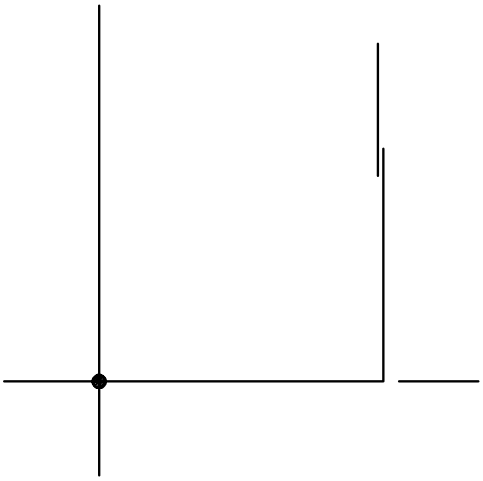
For rectifiers and zeners the region at the knee may display a secondary trace no more than 5 percent of the total voltage of the DUT (see detail).

FIGURE 4023-6. Double trace.



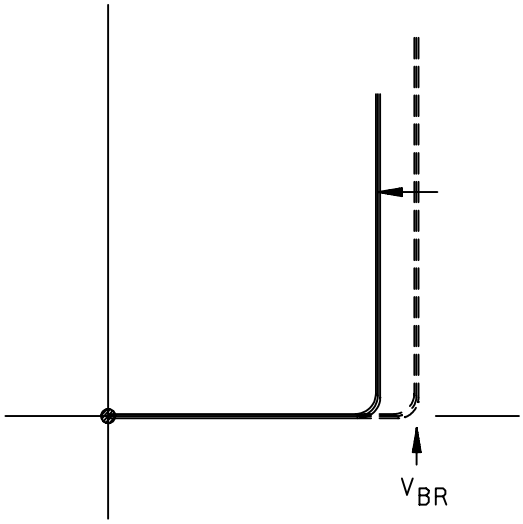
Any jittery movement of the trace in any direction, not caused by power line voltage fluctuations, must not occur.

FIGURE 4023-7. Unstable (jitter).



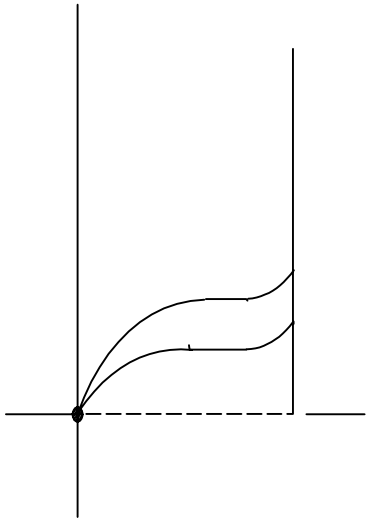
The vertical component must not depart from a single vertical line, except as allowed on figures 4023-5 and 4023-6.

FIGURE 4023-8. Discontinuity.



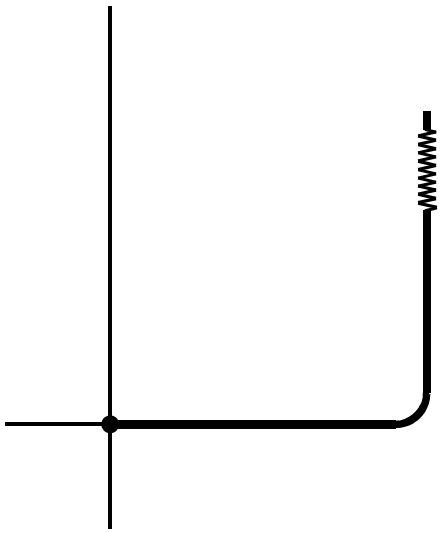
The vertical component must not decrease its value abruptly by 2 percent or more of V_{BR}.

FIGURE 4023-9. Snap back - collapsing V_{BR}



Leakage current (vertical) must not degrade from an initial value.

FIGURE 4023-10. Floater.



Instability (arcing) appearing at or near the specified I_{BR} region on the vertical trace (such as may be coincident with visible sparking activity within the device die region) must not be present. Noise at or near the knee is permissible, such as typically observed on avalanche-zener devices.

FIGURE 4023-11. Arcing.