NOTE: The cover page of this standard has been changed for administrative reasons. There are no other changes to this document.

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30 SEPTEMBER 1985

SUPERSEDING
MIL-STD-188-114
24 MARCH 1976

DEPARTMENT OF DEFENSE INTERFACE STANDARD

ELECTRICAL CHARACTERISTICS OF DIGITAL INTERFACE CIRCUITS

TCTS

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DEPARTMENT OF DEFENSE
Washington, DC 20301

Electrical Characteristics
of Digital Interface Circuits
MIL-STD-188-114A

1. This Military Standard is approved and mandatory for use by all Departments and Agencies of the Department of Defense, in accordance with the memorandum of the Under Secretary of Defense for Research and Engineering, dated 16 August 1983. (See Appendix A).

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to:

Commander
U.S. Army Communications-Electronics Command
ATTN: AMSEL-SEI-I
Fort Monmouth, New Jersey 07703-5203

by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

FOREWORD

1. Originally, Military Standard 188 (MIL-STD-188) covered technical standards for tactical and long haul communications, but later evolved through revisions (MIL-STD-188A, MIL-STD-188B) into a document applicable to tactical communications only (MIL-STD-188C).

2. The Defense Communications Agency (DCA) published DCA Circulars (DCAC) promulgating standards and engineering criteria applicable to the long haul Defense Communications System (DCS) and to the technical support of the National Military Command System (NMCS).

3. As a result of a Joint Chiefs of Staff (JCS) action, standards for all military communications are now being published in a MIL-STD-188 series of documents. The MIL-STD-188 series is subdivided into a MIL-STD-188-100 series covering common standards for tactical and long haul communications, a MIL-STD-188-200 series covering standards for tactical communications only, and a MIL-STD-188-300 series covering standards for long haul communications only. Emphasis is being placed on developing common standards for tactical and long haul communications published in the MIL-STD-188-100 series.

4. This document contains electrical and functional characteristics of the unbalanced and balanced voltage digital interface circuits applicable to both long haul and tactical communications.

5. This document supersedes MIL-STD-188-114 which superseded subparagraph 4.3.1.3 of MIL-STD-188-100 and subparagraph 7.2.1 of MIL-STD-188C.

IDENTIFICATION OF INTERNATIONAL STANDARDIZATION AGREEMENT

Certain provisions of this document (see 4.7) are the subject of international standardization agreement QSTAG 594. When an amendment, revision, or cancellation of this standard is proposed which will modify the international agreement concerned, the preparing activity will take appropriate action through international standardization channels, including departmental standardization offices to change the agreement or make other appropriate accommodations.

ACKNOWLEDGEMENT

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CONTENTS

FIGURES

TABLES

APPENDICES

1. SCOPE

1.1 Purpose. This document specifies the electrical characteristics of the unbalanced voltage and the balanced voltage digital interface circuits, normally implemented in integrated circuit (IC) technology. These circuits shall be employed for the interchange of serial digital binary signals between and among Data Terminal Equipment (DTE) and Data Circuit Terminating Equipment (DCE) or in any interconnection of binary signals between physically separated equipment, regardless of the type of information, such as digitized voice or data, that is represented by the binary signals.

The technical parameters promulgated by this document represent, in general, minimum interoperability and performance characteristics which may be exceeded in order to satisfy specific requirements. Additional nonstandard interface characteristics may also be implemented to satisfy specific interoperability requirements, provided that a basic capability exists to interoperate with a standard interface as stated in this document.

This document does not specify other characteristics of the DTE/DCE interface, such as signal quality, and clock/data phase relationship, essential for satisfactory operation of the interconnected equipment. Those standards are contained in MIL-STD-188-100 and MIL-STD-188-200.

1.2 Application. This document shall be used in the design, installation, and operation of new communications facilities for both the long haul and tactical systems. This document shall be applicable to data, timing or clock, and control circuits employed at the interface between equipment where the information being conveyed is in the form of binary signals at the direct current (dc) baseband level. This document shall also be applicable to alarm and control circuits that are not directly related to data or timing.

This document shall apply to teletypewriters, data terminals, the dc side of signal conversion equipment, both terminal and line side of cryptographic or cryptographic control equipment, digitized voice equipment, and remotely operated equipment where the interface is at the dc baseband. This document shall be applicable at all signaling rates regardless of the type of transmission medium used, e.g., a nominal 4 kilohertz (kHz) channel derived by frequency division multiplexing (FDM), a nominal 48 kHz channel derived by FDM, a channel derived by time division multiplexing (TDM), or a fiber optic or metallic wire connection. Figure 1 depicts a block diagram of a data terminal subsystem as an example to illustrate where the digital interface applies. Figure 1 shows data and timing circuits but does not show control circuits.

Any or all of the equipment of the terminal subsystem may be integrated and combined in a single piece of equipment. When combined in a single piece of equipment, this document does not apply to internal equipment connections.

Information on the interrelationship of this document with FED-STD-1020A, FED-STD-1030A and other low level digital interface standards is given in Appendix D.

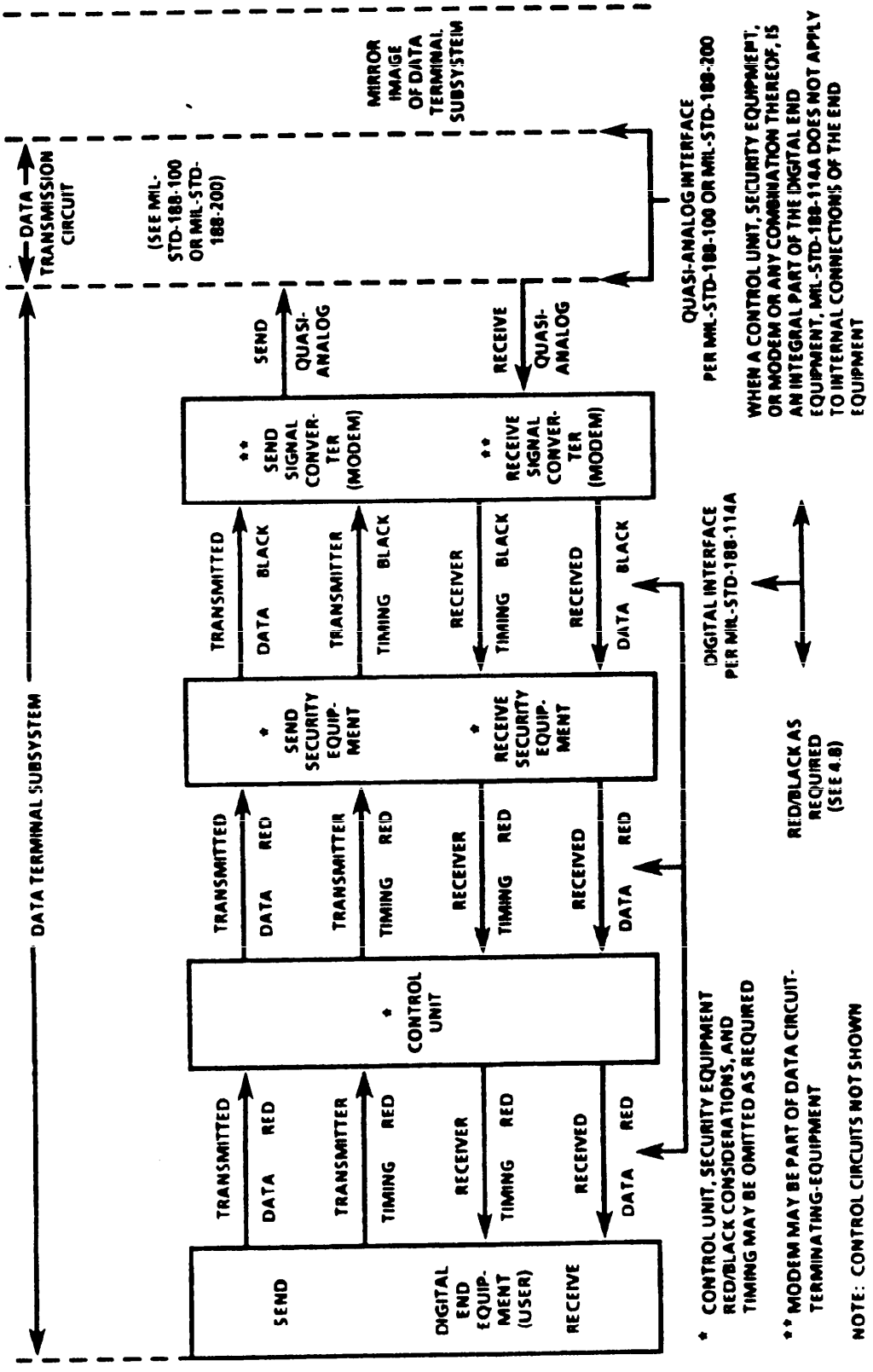


FIGURE 1. Block diagram of data terminal subsystem.

This document does not apply to digital transmission subsystems employing specialized non-binary waveforms for transmission. Standards for these types of subsystems are under consideration and will be published in another document of the MIL-STD-188 series.

It is not intended that existing equipment and facilities be immediately converted to comply with the requirements of this document. New systems and those systems undergoing major modification or rehabilitation shall comply with the standards contained in this document subject to the applicable requirements of current procurement regulations.

1.3 System standards and design objectives. The parameters and other requirements specified in this document are mandatory system standards (see Appendix A) if the word "shall" is used in connection with the parameter value or requirement under consideration. Nonmandatory design objectives are indicated by parentheses after a standardized parameter value or by the word "should" in connection with the parameter value or requirement under consideration. For a definition of the terms "System Standard" and "Design Objective" see Federal Standard (FED-STD) 1037.

2. REFERENCED DOCUMENTS

2.1 Government documents.

2.1.1 Standards. Unless otherwise specified, the following standards of the issue of the Department of Defense Index of Specifications and Standards (DoDISS) specified in the solicitation form a part of this standard to the extent specified herein.

STANDARDS

FEDERAL

FED-STD-1037	Glossary of Telecommunication Terms

MILITARY

MIL-STD-188-100	Common Long Haul and Tactical Communication System Technical Standards
MIL-STD-188-124	Grounding, Bonding and Shielding for Common Long Haul/Tactical Communication Systems
MIL-STD-188-200	System Design and Engineering Standards for Tactical Communications

2.1.2 Other Government documents and publications. The following other Government documents and publications form a part of this standard to the extent specified herein.

NACSIM 5100, Compromising Emanations Laboratory Test Requirements, Electromagnetics (U)

Quadripartite Standardization Agreement (QSTAG)

QSTAG-594	Electrical Characteristics of Digital Interface Circuits

(Copies of specifications, standards, handbooks, drawings, and publications required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this standard and the references cited herein, the text of this standard shall take precedence.

3. DEFINITIONS

3.1 Definitions. Definition of terms used in this document shall be as specified in FED-STD-1037.

3.2 Abbreviations and acronyms. Abbreviations and acronyms used in this document are listed in Appendix B.

4. GENERAL REQUIREMENTS

4.1 Description of digital interface circuits. The interface circuits consist of a generator connected by an interconnecting wire or cable to a load. The load is comprised of one or more receivers and a termination resistor, where applicable. The electrical characteristics of the digital interface circuits are specified in terms of required voltage, current and resistance values obtained from direct measurement of the generator and receiver components. The generator characteristics for the unbalanced voltage digital interface circuit are electrically different from the generator characteristics for the balanced voltage digital interface circuits, whereas the receiver characteristics are electrically identical for both the unbalanced and the balanced voltage digital interface circuits. Guidance is given in Appendix C concerning the characteristics of the interconnecting wire or cable and with respect to limitations on signaling rates imposed by the parameters of wire or cable length, balance, termination, and generation of near-end crosstalk, where applicable. Information on the interrelation of this document with other low level digital interface standards is given in Appendix D. The requirements for signal waveshaping, generally necessary to reduce unbalanced circuit near-end crosstalk to adjacent circuits, are also described. For the purpose of this document, the terms interface circuit and interchange circuit are considered to be identical.

4.2 Description of functional interchange circuits. Functional interchange circuits are used to connect DTE and DCE for the purpose of exchanging data and timing signals and to control the flow of information. Flow control may be extended from one DTE through one or more DCE to another DTE on an end-to-end basis by appropriate communications protocols. Functional interchange circuits may be subdivided into four general classes:

Data (send and receive)
Timing or clock (send and receive)
Control (including status, indicator and alarm),
Ground or common return.

Connectors, pin assignments and communications protocols are not standardized in this document.

4.3 Signaling rate range. The unbalanced voltage digital interface circuit (see 5.1) can generally be utilized on data, timing or clock, and control circuits where the signaling rate on these circuits is up to 100 kilobits per second (kb/s). The balanced voltage digital interface circuit (see 5.2) can generally be utilized on data, timing or clock, and control circuits where the signaling rate on these circuits is up to 10 megabits per second (Mb/s). The terminated voltage digital interface circuit (see 5.3) can generally be utilized on data, timing or clock, and control circuits where the signaling rate on these circuits exceeds 10 Mb/s.

Digital interface devices meeting the electrical characteristics of this document need not operate over the entire signaling rate range indicated above. The devices may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower signaling rates.

4.4 Selection of type of digital interface circuit. The choice of either the balanced or the unbalanced voltage digital interface circuit is left to the designer and depends upon the signaling rate, the distance between generator and load, noise and grounding conditions, and other factors.

4.4.1 Types of balanced generators. Three different types of generators may be used for the balanced voltage digital interface circuit. All three types of balanced generators use the same type of receiver used with unbalanced generators. The three types of balanced generators are as follows:

The type I generator has an offset voltage of not more than 0.4 volts and is intended to be used for balanced interfaces operating at signaling rates below 100 kb/s. The low offset voltage is necessary for interoperability with older military digital equipment. (See 4.5.) The type I generator corresponds to the original MIL-STD-188-114 balanced generator.

The type II generator has an offset voltage of up to three volts and corresponds to the FED-STD-1020A and EIA RS-422A balanced generators. The type II generator is intended to be used for balanced interfaces operating at signaling rates between 100 kb/s and 10 Mb/s where no interoperability requirements with older military digital equipment is expected to exist.

The type III generator is a new terminated voltage generator and is intended to be used for balanced voltage digital interface circuits operating at signaling rates over 10 Mb/s.

4.4.2 Use of balanced voltage digital interface circuit. While the balanced voltage digital interface circuit is intended for use at higher signaling rates than the unbalanced voltage digital interface circuit, the general use of the balanced voltage digital interface circuit is recommended where any of the following conditions prevail:

a. The interconnecting wire or cable is too long for effective unbalanced operation.

b. The interconnecting wire or cable is exposed to extraneous noise sources that may cause an unwanted voltage in excess of plus or minus one volt measured differentially between the signal conductor and circuit common ground at the load end of the wire or cable with a 50-ohm resistor substituted for the generator.

c. It is necessary to minimize interference with other signals.

d. Inversion of signal sense of the transmitted signal may be required, e.g., plus MARK to minus MARK may be obtained by inverting the wire or cable pair of the balanced generator. (See Figure 29.)

4.4.3 Use of balanced and unbalanced voltage digital interface circuits. The parameter values for the generator and load components of the interface are designed such that balanced and unbalanced voltage digital interface circuit connections may be carried in the same cable. For example, the balanced voltage digital interface circuits may be used for data and timing while the unbalanced voltage digital interface circuits may be used for control functions operating with lower signaling rates than the data and timing circuits.

4.5 Relationship with other digital interface standards. The parameter values contained in this document are identical to corresponding parameter values of FED-STD-1020A and FED-STD-1030A with the exception of the balanced generator offset voltage V_{os} (see 5.2.1.4) of the type I generator. This deviation is considered essential for interfaces operating at signaling rates below 100 kb/s, in order to ensure compatibility and direct interoperability between new equipment designed in accordance with this document and equipment currently in the inventory designed in accordance with previous standards of the MIL-STD-188 series. The term "direct interoperability" should be understood to mean that no modification of low level digital interface equipment is required and no additional device is needed for satisfactory exchange of information between older and new low level digital interface equipment.

The type II generators are intended for interfaces operating at signaling rates between 100 kb/s and 10 Mb/s, which are not expected to interface with older equipment designed in accordance with previous standards of the MIL-STD-188 series. The 0.4 volts offset voltage specified in this document for the type I generator is a more stringent subset and falls completely within the specifications of FED-STD-1020A.

4.6 Grounding requirements. Grounding of digital interface circuits shall comply with the applicable requirements of the current edition of MIL-STD-188-124.

NOTE: Optional grounding arrangements are contained in 30.6 of Appendix C.

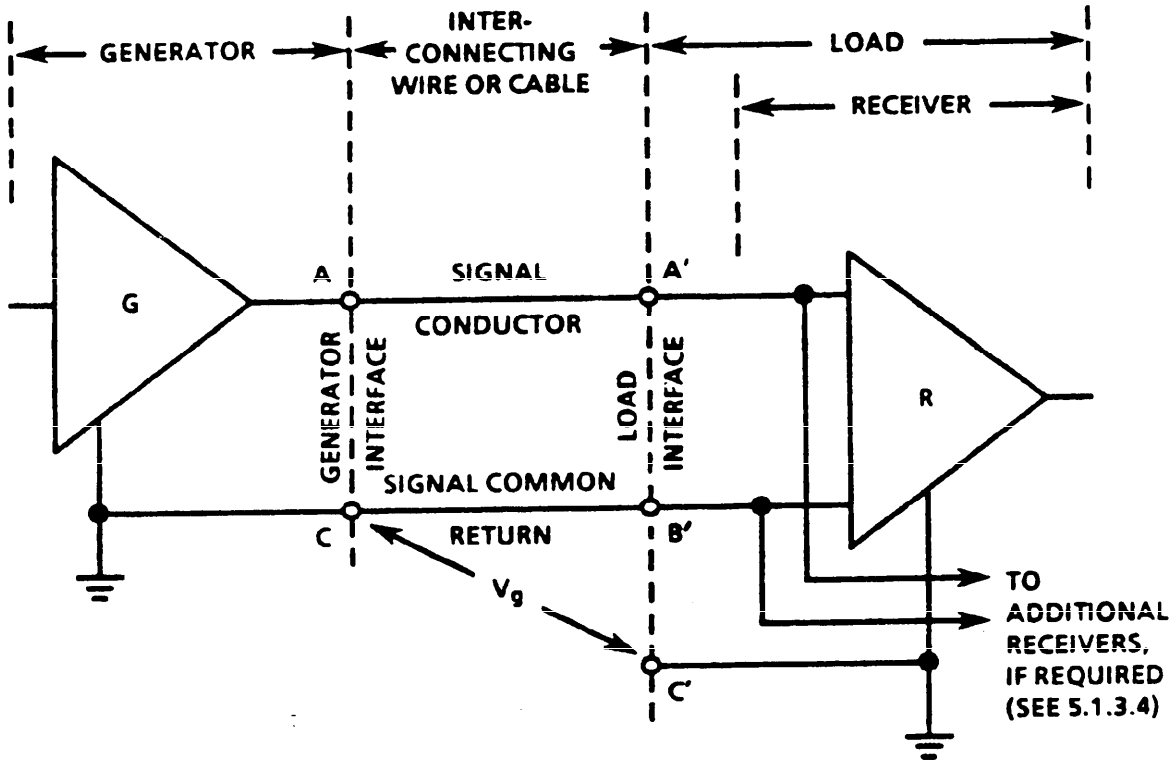
4.7 Interoperability requirements of ABCA Armies. The electrical characteristics for binary signals at an interface for the exchange of digital information among American, British, Canadian and Austrialian (ABCA) Armies or Forces shall comply with the applicable requirements of the current edition of QSTAG 594.

NOTE: The requirements of this document are compatible with the requirements

4.8 Compromising emanations (TEMPEST) requirements. Digital interface circuits requiring TEMPEST protection shall comply with the applicable requirements of the current edition of the NACSIM 5100 series.

5. DETAILED REQUIREMENTS

5.1 Unbalanced voltage digital interface circuit. The unbalanced voltage digital interface circuit is shown in Figure 2. The circuit consists of three parts: the generator (G), the interconnecting wire or cable, and the load. The load consists of one or more receivers (R) (see 5.1.3.4). The electrical characteristics of the generator and the receiver are specified in terms of direct electrical measurements. Guidance is provided in 30.3 of Appendix C regarding the electrical and physical characteristics of the interconnecting wire or cable.



LEGEND:

A, C - GENERATOR INTERFACE POINTS

C - GENERATOR CIRCUIT GROUND

A', B' - LOAD INTERFACE POINTS

C' - LOAD CIRCUIT GROUND

V_g - GROUND POTENTIAL DIFFERENCE

FIGURE 2. Unbalanced voltage digital interface circuit.

5.1.1 Generator characteristics. The electrical characteristics of the unbalanced generator are specified in accordance with measurements illustrated in Figures 3 through 6 and described in 5.1.1.1 through 5.1.1.9. The measurements are under static conditions, whereas measurements under dynamic conditions are not standardized. A generator meeting these requirements results in a low impedance (50 ohms or less) unbalanced voltage source that will produce a voltage applied to the interconnecting wire or cable in the range of 4 volts to 6 volts.

5.1.1.1 Signal sense. The signal sense of the generator output voltages appearing across the interconnecting wire or cable (see Figure 2) shall be as shown in Table I.

TABLE I. Signal sense for unbalanced generators.

VOLTAGE POLARITY (See Figure 2)	DATA	TIMING	CONTROL and ALARM
Point A negative with respect to point C	1 or MARK	OFF (QUIESCENT)	OFF
Point A positive with respect to point C	0 or SPACE	ON (ACTIVE)	ON

NOTE: The MARK and SPACE states for telegraphy and data transmission have been changed from positive MARK and negative SPACE (MIL-STD-188-100, subparagraph 4.3.1.5) to negative MARK and positive SPACE. It is not intended that existing equipment and facilities be converted to the negative MARK/positive SPACE states unless a major facility modification or rehabilitation is planned and such conversion could be accommodated during that work. It is, however, intended that new procurement of equipment and facilities will insure that a provision for negative and positive MARK is accommodated. This does not mean that negative MARK will necessarily be implemented immediately simply because the equipment or facility is new. This guidance is only intended to mean that new equipment or facilities will be purchased with the positive and negative MARK capability and the facilities engineering or operating agency will be expected to make the necessary decisions to change to negative MARK on a case by case basis, subject to operational and fiscal constraints.

5.1.1.2 Signaling rate range. Not standardized. (See Appendix C)

5.1.1.3 Open-circuit measurement. (See Figure 3.) For either binary state, the magnitude of the voltage (V_o) measured between the generator output terminal A and generator circuit ground (terminal C) shall not be less than 4 volts nor more than 6 volts. For the opposite binary state, the polarity of V_o shall be reversed ($\bar{V}_o$).

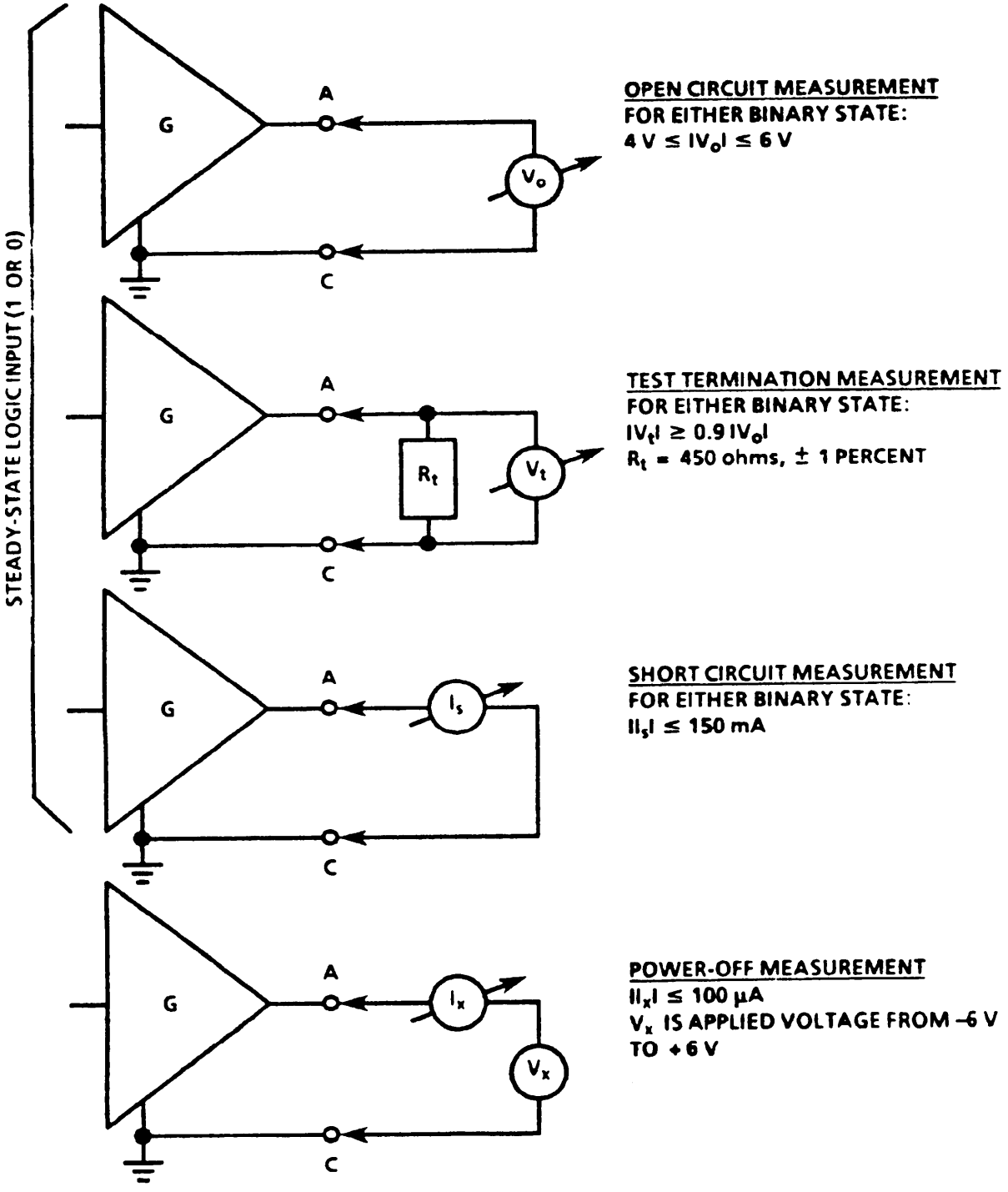
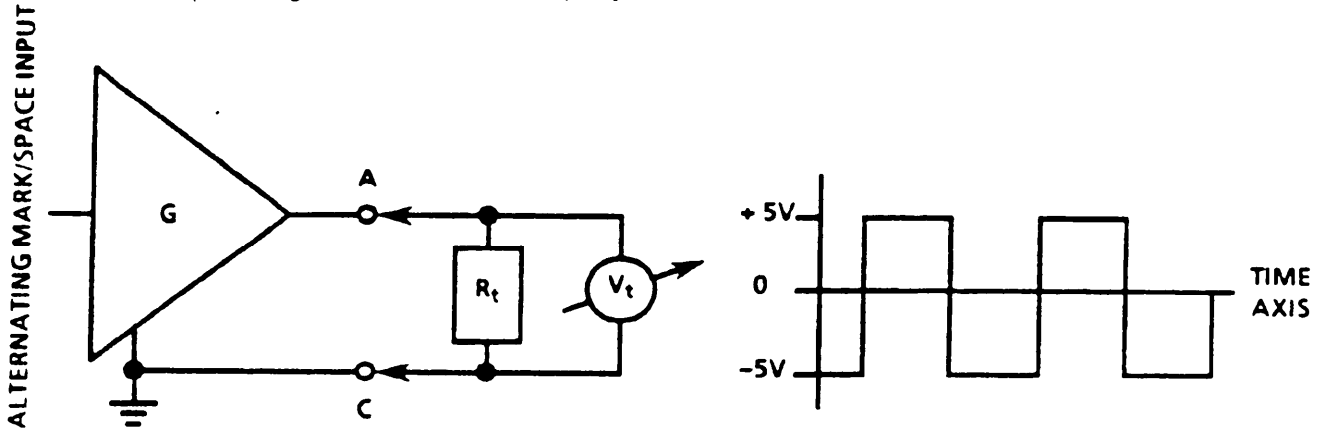


FIGURE 3. Unbalanced generator parameter measurements.

5.1.1.4 Test termination measurement. (See Figure 3.) With a test load of 450 ohms ±1 percent connected between the generator output terminal A and generator circuit ground (terminal C), the magnitude of the voltage (V_t) measured between the generator output terminal A and generator circuit ground (terminal C) shall not be less than 90 percent of the magnitude of V_o for one binary state. For the opposite binary state, the polarity of V_t shall be reversed ($\overline{V}_t$) and $\overline{V}_t$ shall not be less than 90 percent of the magnitude of $\overline{V}_o$.

NOTE: A nominal voltage waveform for alternating binary states is shown in Figure 4. This waveform is intended to represent a typical unbalanced generator output signal, such as displayed on an oscilloscope.



LEGEND: V_t = 5 V (ASSUMED VALUE)
R_t = 450 ohms

FIGURE 4. Nominal waveform of unbalanced generator.

5.1.1.5 Short-circuit measurement. (See Figure 3.) With the generator output terminal A short-circuited to generator circuit ground (terminal C), the magnitude of the current I_s flowing through the generator output terminal A shall not exceed 150 milliamperes (mA) for either binary state.

5.1.1.6 Power-off measurement. (See Figure 3.) Under power-off conditions, the magnitude of the generator output leakage current (I_x), with a voltage V_x ranging between +6 volts and -6 volts applied between the generator output terminal A and generator circuit ground (terminal C), shall not exceed 100 microamperes.

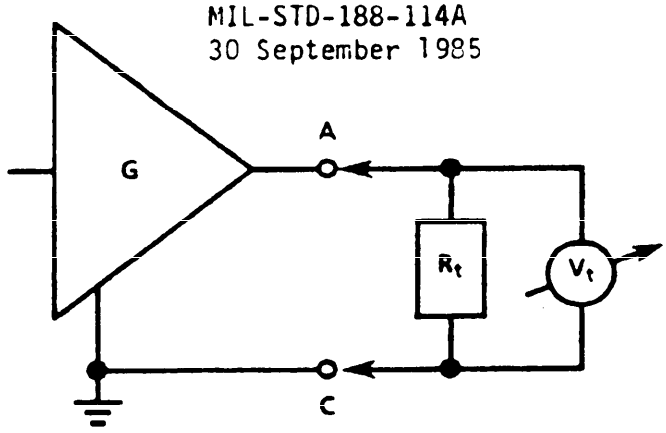
5.1.1.7 Output signal waveform. (See Figure 5.) During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the signal measured across a 450 ohms ±1 percent test load connected between the generator output terminal A and generator circuit ground (terminal C) shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{ss}. Thereafter, the signal voltage shall not vary more than 10 percent of V_{ss} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of V_t or $\overline{V}_t$ exceed 6 volts, nor be less than 3.6 volts. V_{ss} is defined as the voltage difference between the two terminated steady state values V_t and $\overline{V}_t$ of the generator output.

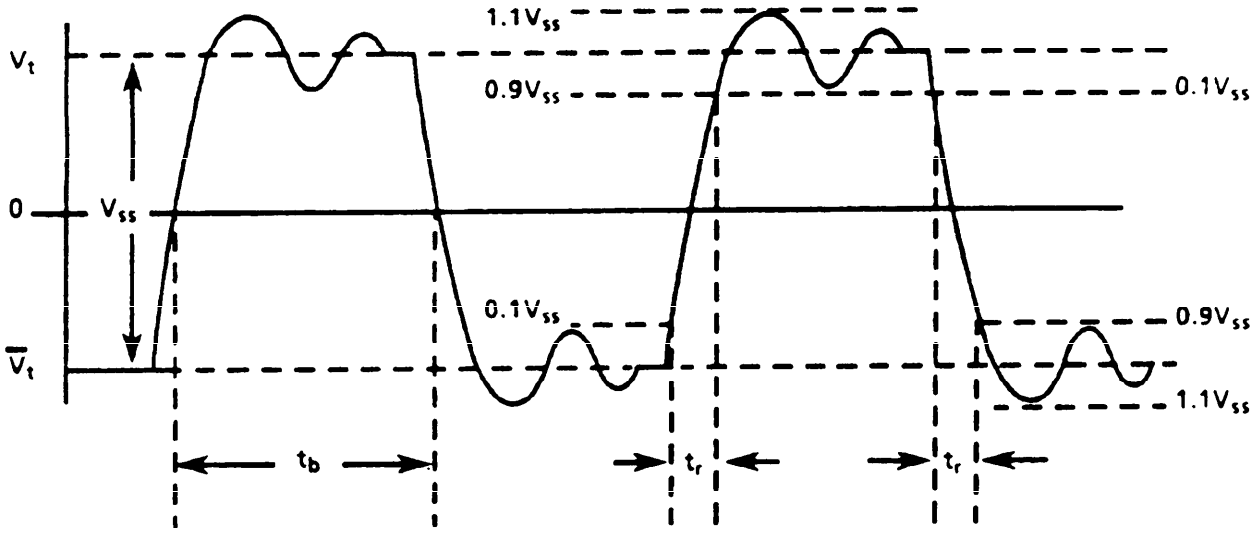
5.1.1.8 Output signal waveshaping. (See Figure 5.) Waveshaping of the generator output signal shall be employed to control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The rise time t_r of the signal shall be controlled to ensure that the signal reaches 0.9 V_{ss} between 0.1 and 0.3 of the unit interval (t_b) at the maximum signaling rate. Below 1 kb/s, t_r shall be between 100 microseconds and 300 microseconds. The method of providing the waveshaping is not standardized, but examples are given in Note 3, below.

NOTE 1: The near-end crosstalk is a function of both rise time and wire or cable length (see 30.3.5 of Appendix C) and, therefore, in establishing the standard for waveshaping, both of these characteristics have been considered.

NOTE 2: If a generator is to operate over a range of signaling rates and employs a fixed amount of waveshaping which meets the standard for the maximum signaling rate of the operating range, the waveshaping is considered adequate for all lesser signaling rates and equal or lesser cable lengths recommended for the maximum signaling rate in Figure 18 of Appendix C, even though this may result in a rise time less than 0.1 t_b for the actual operating rate.

NOTE 3: The required waveshaping may be accomplished, for example, either by providing a slew rate control in the generator or by inserting an RC filter at the generator interface point. A combination of these methods may also be employed. Care should be taken to prevent oscillations which may be caused by slew rate control circuitry. The designer is cautioned that the use of internal generator waveshaping controls provided by some manufacturers may give rise to instability during generator transitions. Measured results of this instability have revealed burst oscillations in the gigahertz (GHz) frequency range which can cause faulty equipment operation. For this reason, until a solution has been found, the preferred waveshaping technique is the external RC network. An example of the RC filter method is shown in Figure 6. Typical values of capacitance C_w, with the value of R_w selected so that R_w plus the output resistance of the generator is approximately 50 ohms, that

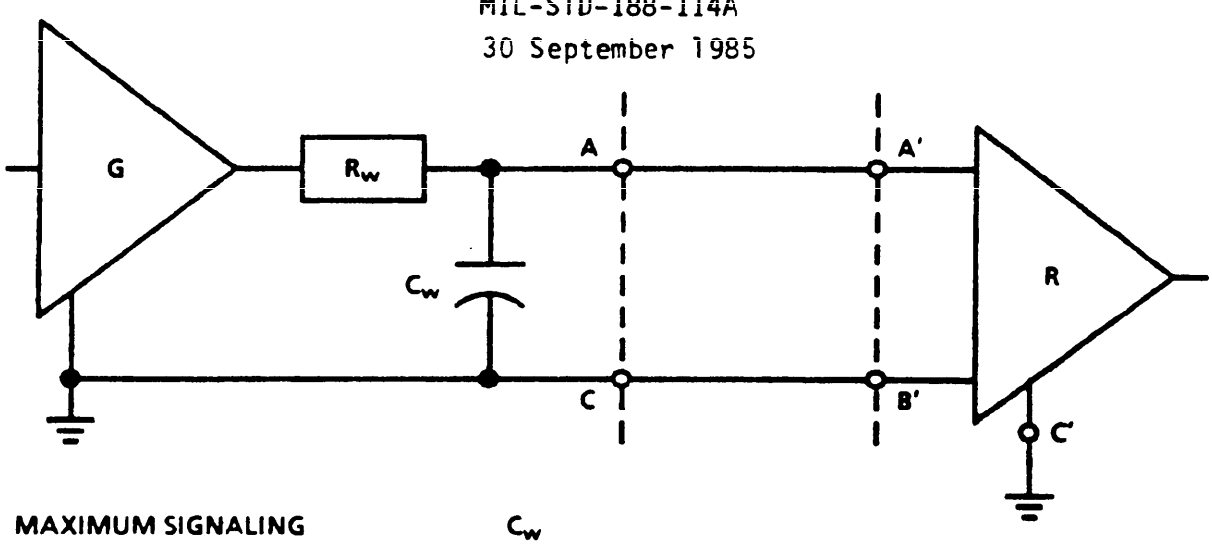




LEGEND: R_t = 450 ohms ± 1 PERCENT
$|V_{ss}|$ = $|V_t - \overline{V}_t|$
V_{ss} = DIFFERENCE IN STEADY STATE VOLTAGES
t_b = UNIT INTERVAL
t_r = 100 µ TO 300 µs WHEN $t_b \geq$ 1ms
t_r = 0.1t_b TO 0.3 t_b WHEN $t_b <$ 1 ms

FIGURE 5. Unbalanced generator output signal waveform.

may be employed with typical twisted pair cable are also given. These values apply for operating distances from zero to that shown by the curve in Figure 18 of Appendix C for the applicable signaling rate. Where generators are driving clock leads, the same waveshaping design may be employed as used on the associated data leads. If the clock signaling rate is directly related to the data signaling rate, one half of the period of the clock should be used in lieu of t_b to determine rise time. (See also subparagraph 4.3.1.6 of MIL-STD-188-100 and subparagraph 5.3.6 of MIL-STD-188-200).



MAXIMUM SIGNALING RATE (kb/s)	C_w (MICROFARADS)
0 - 2.5	1.0
2.5 - 5	0.47
5 - 10	0.22
10 - 25	0.10
25 - 50	0.047
50 - 100	0.022

R_w IS APPROXIMATELY 50 ohms MINUS THE GENERATOR OUTPUT RESISTANCE

FIGURE 6. Example method for waveshaping of unbalanced voltage digital interface circuit.

5.1.1.9 High impedance output state. The generator output should be permitted to assume a high impedance state, if required for multiple generator bus operation. If a high impedance state is implemented, the output voltage shall be nominally zero for the high impedance state when measured with a test termination as stated in 5.1.1.4.

5.1.2 Wire or cable characteristics. Not standardized.

NOTE: Guidelines on wire or cable characteristics are given in 30.3 of Appendix C.

5.1.3 Load characteristics. The load consists of one or more receivers (R) as shown in Figure 2. The electrical characteristics of a single receiver without fail safe provision are specified in terms of the measurements illustrated in Figures 7 through 9 and described in 5.1.3.1 through 5.1.3.3. A device meeting these requirements results in a differential receiver having a high input impedance (4000 ohms or more), a small input threshold transition region between -0.2 volts and +0.2 volts, and allowance for an internal bias voltage not to exceed 3 volts in magnitude. Multiple receivers and a provision for fail safe operation for specific applications are allowed in the load within the limitations specified in 5.1.3.6. The receiver used in the load for the unbalanced voltage digital interface circuit is electrically identical to the receiver for the balanced voltage digital interface circuits stated in 5.2 and 5.3.

5.1.3.1 Receiver input current-voltage measurement. (See Figure 7.) With the voltage V_{ia} (or V_{ib}) ranging between -10 volts and +10 volts, while V_{ib} (or V_{ia}) is held at 0 volts (grounded), the resultant input current I_{ia} (or I_{ib}) shall remain within the shaded region shown in the graph in Figure 8. These measurements shall be made with the power supply (or supplies) of the receiver in both the power-on and power-off conditions.

5.1.3.2 Receiver input sensitivity measurement. (See Figure 8.) Over an entire common mode voltage (V_{cm}) range of -7 volts to +7 volts, the receiver shall require a differential input voltage V_i of not more than 200 millivolts (mV) to correctly assume the intended binary state. The common mode voltage V_{cm} is defined as the algebraic mean of the two voltages appearing at the receiver input terminals A' and B' with respect to the receiver circuit ground C'. Reversing the polarity of V_i shall cause the receiver to assume the opposite binary state. The receiver is required to maintain correct operation for differential input signal voltages ranging between 200 mV and 6 volts in magnitude. The maximum voltage (signal plus common mode) present between either receiver input terminal and receiver circuit ground shall not exceed 10 volts in magnitude and shall not cause the receiver to operationally fail. Additionally, the receiver shall tolerate the conditions specified in 5.1.5 without being damaged.

NOTE: Designers of terminating hardware should be aware that slow signal transitions with noise present may give rise to instability or oscillatory conditions in the receiver and, therefore, appropriate techniques should be implemented to prevent such behavior. For example, adequate hysteresis may be incorporated into the receiver to prevent such conditions.

5.1.3.3 Receiver input balance measurement. (See Figure 9.) The balance of the receiver input voltage-current characteristics and bias voltages shall be such that the receiver will remain in the intended binary state when a differential voltage (V_i) of 400 mV is applied through resistors of 500 ohms ±1 percent to each input terminal A' and B', as shown in Figure 9, and V_{cm} is varied between -7 volts and +7 volts. When the polarity of V_i is reversed, the opposite binary state shall be maintained under the same conditions.

5.1.3.4 Multiple receivers. Not standardized.

NOTE: The use of up to ten receivers in the load may be optionally employed. However, extreme caution must be exercised to avoid performance degradation due to signal reflections from stub lines emanating from the load interface point to the receivers. See 5.1.3.6 for limits on total load resistance and sensitivity.

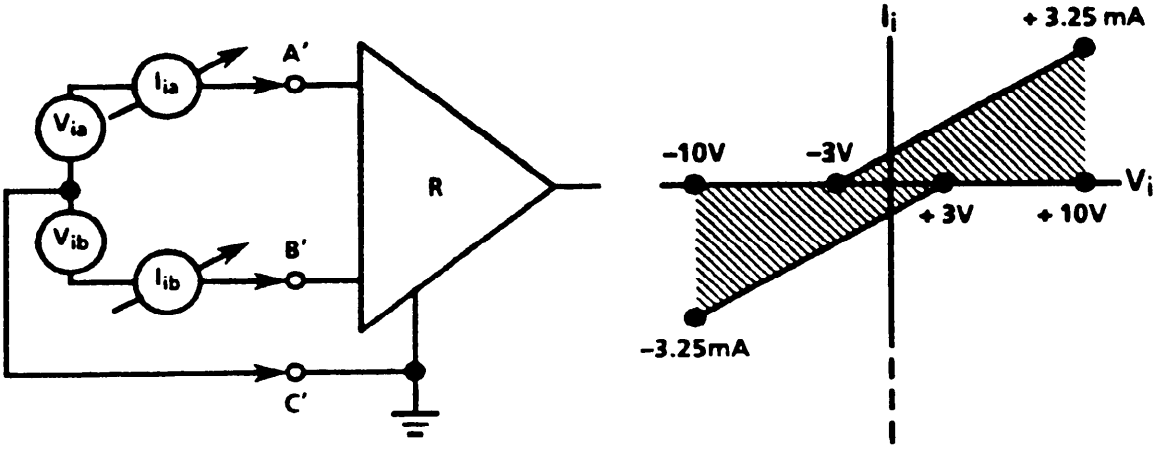


FIGURE 7. Receiver input current-voltage measurement.

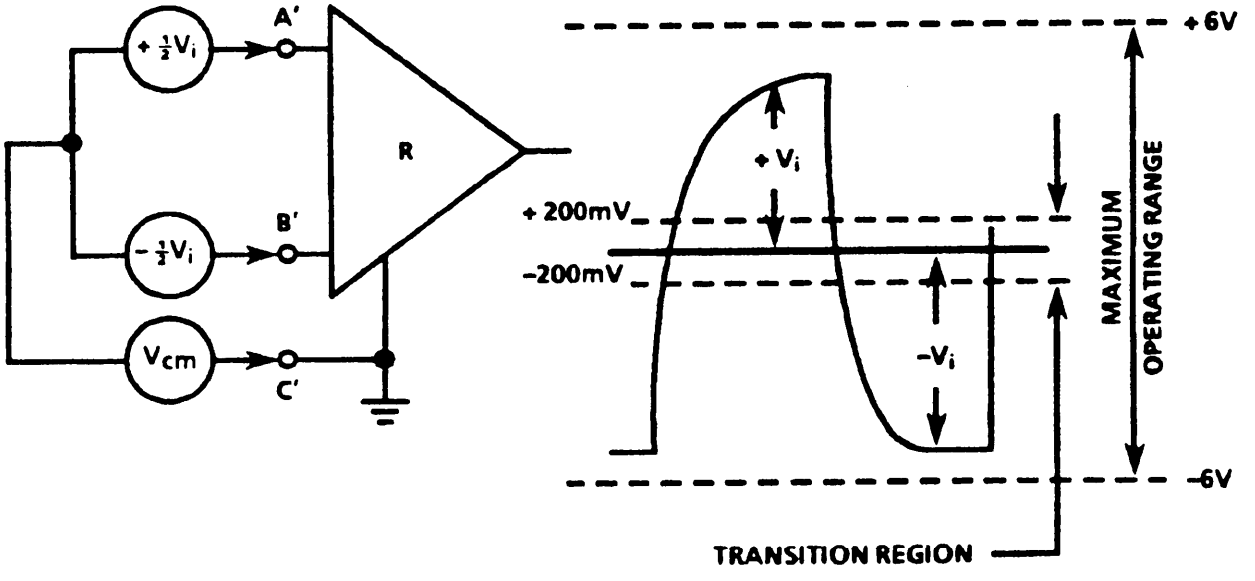
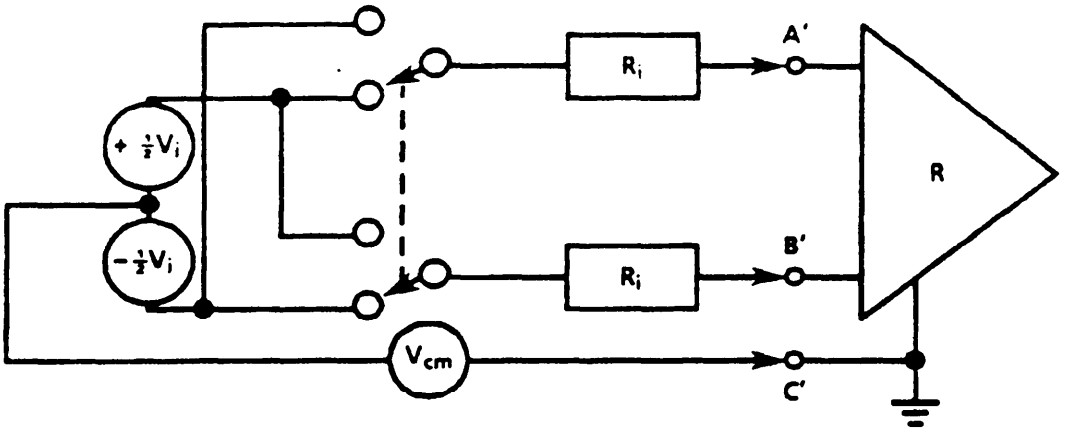


FIGURE 8. Receiver input sensitivity measurement.



LEGEND: V_{cm} = -7 V TO +7 V
V_i = 400 mV
R_i = 500 ohms, ± 1 PERCENT

FIGURE 9. Receiver input balance measurement.

5.1.3.5 Fail safe operation. Where a fail safe is required, a provision shall be incorporated in the load to provide a steady binary condition (either MARK or SPACE as required by the application) to protect against certain fault conditions.

NOTE: The method of providing fail safe is not standardized. An example of fail safe operation is given in 30.5.1 of Appendix C.

5.1.3.6 Total load characteristic limits. The total load including multiple receivers and fail safe provisions shall have a resistance greater than 400 ohms between its input points (terminals A' and B' of Figure 2) and shall require a differential input voltage of not more than 200 mV for all receivers to assume the intended binary state.

5.1.4 Operational constraints. An unbalanced voltage digital interface circuit conforming to 5.1 will perform satisfactorily at signaling rates up to 100 kb/s providing that the following operational constraints are simultaneously satisfied:

a. The interconnecting wire or cable length is within that recommended for the applicable signaling rate indicated in 30.3.5 of Appendix C.

b. The common mode voltage at the receiver is less than 4 volts (peak). The common mode voltage is defined to be any uncompensated combination of generator-receiver ground potential difference, the generator offset voltage (V_{OS}), and longitudinally coupled peak random noise voltage measured between the receiver circuit ground and the wire or cable with the generator ends of the wire or cable short-circuited to ground.

c. The amplitude of the received signal is at least 0.2 volts greater than the total peak noise between the signal conductor and common return at the load interface point, with a 50-ohm resistor substituted for the generator (and waveshaping network, if used) at the generator interface point.

NOTE: Care should be taken when power for distant receivers is supplied in the same or in adjacent conductors as used for data, clock or control signals, in order to avoid performance degradation that may be caused by power supply surges and spurious voltage transients.

5.1.5 Circuit protection. Interface circuit protection shall be provided such that any generator or receiver, under either the power-on or the power-off condition, shall not be damaged by occurrence of any of the following conditions:

a. Voltage magnitudes of 12 volts (Design Objective: 25 volts) on the receiver leads.

b. Shorting of the generator or the receiver terminals to ground or to each other.

c. Crossing of the leads with any other physical leads of the interface circuit.

d. Opening of either or both of the generator or receiver leads.

e. Whenever the generator or receiver is to be connected by a metallic circuit directly to pairs of an outside plant cable, additional protective circuitry shall be provided to protect the generator and receiver against the spurious voltage transients and power surges commonly experienced across a cable pair or between either conductor of a cable pair and ground. The protective circuitry shall be adequate to ensure that the generator or receiver will not be damaged by the appearance across the cable pair or between either conductor and ground, of

(1) a voltage transient of up to 1000 volts peak with a 5 microsecond rise time and decaying to 50 percent of peak voltage in 600 microseconds, and

(2) a voltage transient of up to 350 volts peak with a 10 microsecond rise time and decaying to 50 percent of peak voltage in 2000 microseconds.

NOTE: The faults or conditions listed in 5.1.5 may cause the power dissipation in the interface devices to approach the maximum power dissipation that may be tolerated by a typical IC package. It is therefore cautioned that where multiple generators or receivers are implemented in a single IC package, only one such fault or condition per package may be tolerated at one time without damage occurring to the IC package.

5.2 Balanced voltage digital interface circuit. The balanced voltage digital interface circuit is shown in Figure 10. The circuit consists of three parts: the generator (G) which may be a type I or a type II generator (see 4.4.1), the balanced interconnecting wire or cable, and the load. The load consists of one or more receivers (R) (see 5.2.3.4) and an optional wire or cable termination resistance (R_t). The electrical characteristics of the generator and the receiver are specified in terms of direct electrical measurements. Guidance is provided in 30.3 of Appendix C regarding the electrical and physical characteristics of the interconnecting wire or cable.

5.2.1 Generator characteristics. The electrical characteristics of the balanced generator are specified in accordance with measurements illustrated in Figures 11, 12 and 13 and described in 5.2.1.1 through 5.2.1.8. The characteristics apply to both type I and type II generators (see 4.4.1) unless otherwise stated in the applicable subparagraph. The measurements are under static conditions, whereas measurements under dynamic conditions are not standardized. A generator meeting these requirements results in a low impedance (100 ohms or less) balanced voltage source that will produce a differential voltage applied to the interconnecting wire or cable in the range of 2 volts to 6 volts.

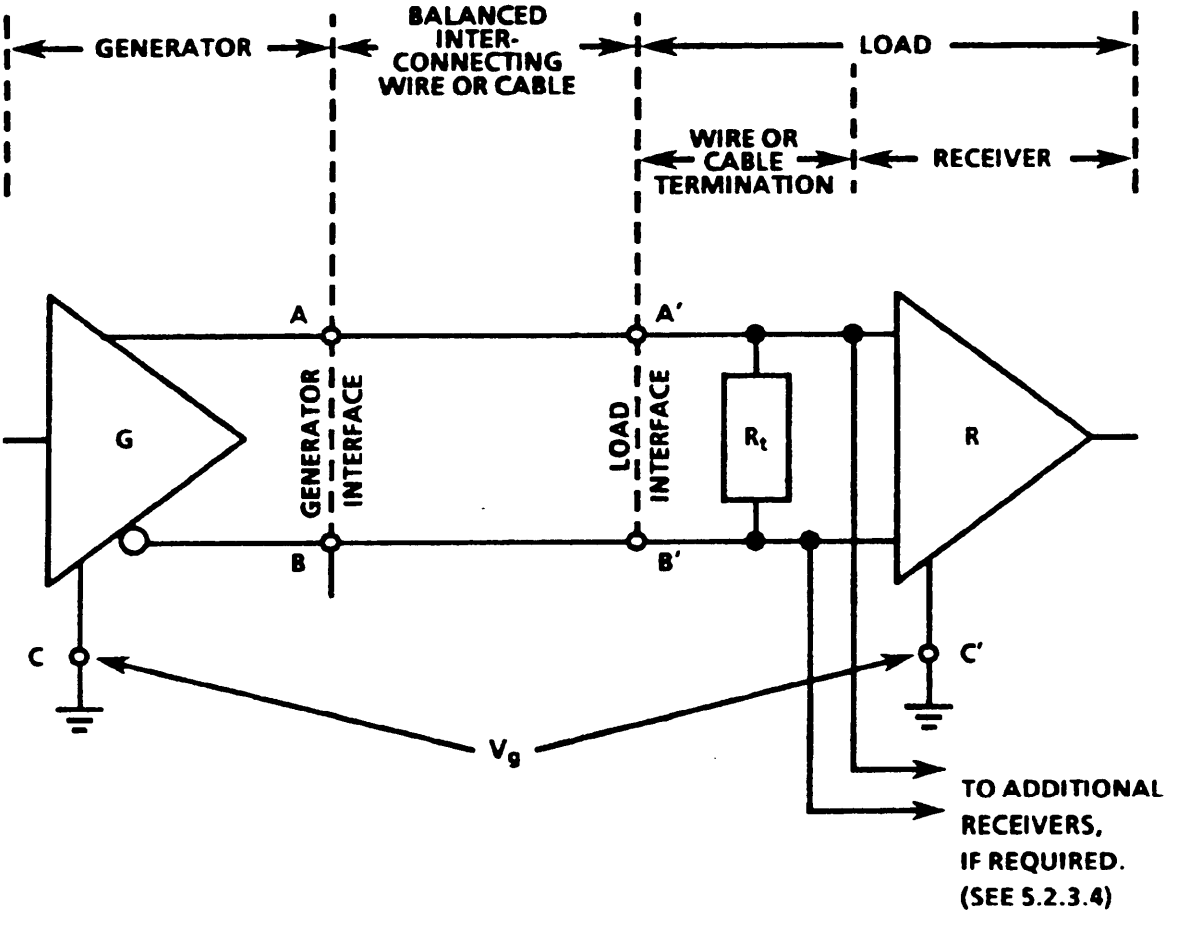
5.2.1.1 Signal sense. The signal sense of the generator output voltages appearing across the interconnecting wire or cable (see Figure 10) shall be as shown in Table II. (See Note of 5.1.1.1.)

TABLE II. Signal sense for balanced generators

VOLTAGE POLARITY (See Figures 10 and 14)	DATA	TIMING	CONTROL and ALARM
Point A negative with respect to point B	1 or MARK	OFF (QUIESCENT)	OFF
Point A negative with respect to point B	0 or SPACE	ON (ACTIVE)	ON

5.2.1.2 Signaling rate range. Not standardized. (See 4.3.)

5.2.1.3 Open-circuit measurement. (See Figure 11.) For either binary state, the magnitude of the differential open-circuit voltage (V_o) measured between the generator output terminals A and B shall not be less than 4 volts nor more than 6 volts. For type I generators, the magnitudes of the open-circuit voltages V_{oa} and V_{ob} measured between the generator output terminals A or B and the generator circuit ground (terminal C) shall not be less than 2 volts nor more than 3 volts. For type II generators, the magnitudes of the



LEGEND:

A, B - GENERATOR INTERFACE POINTS

C - GENERATOR CIRCUIT GROUND

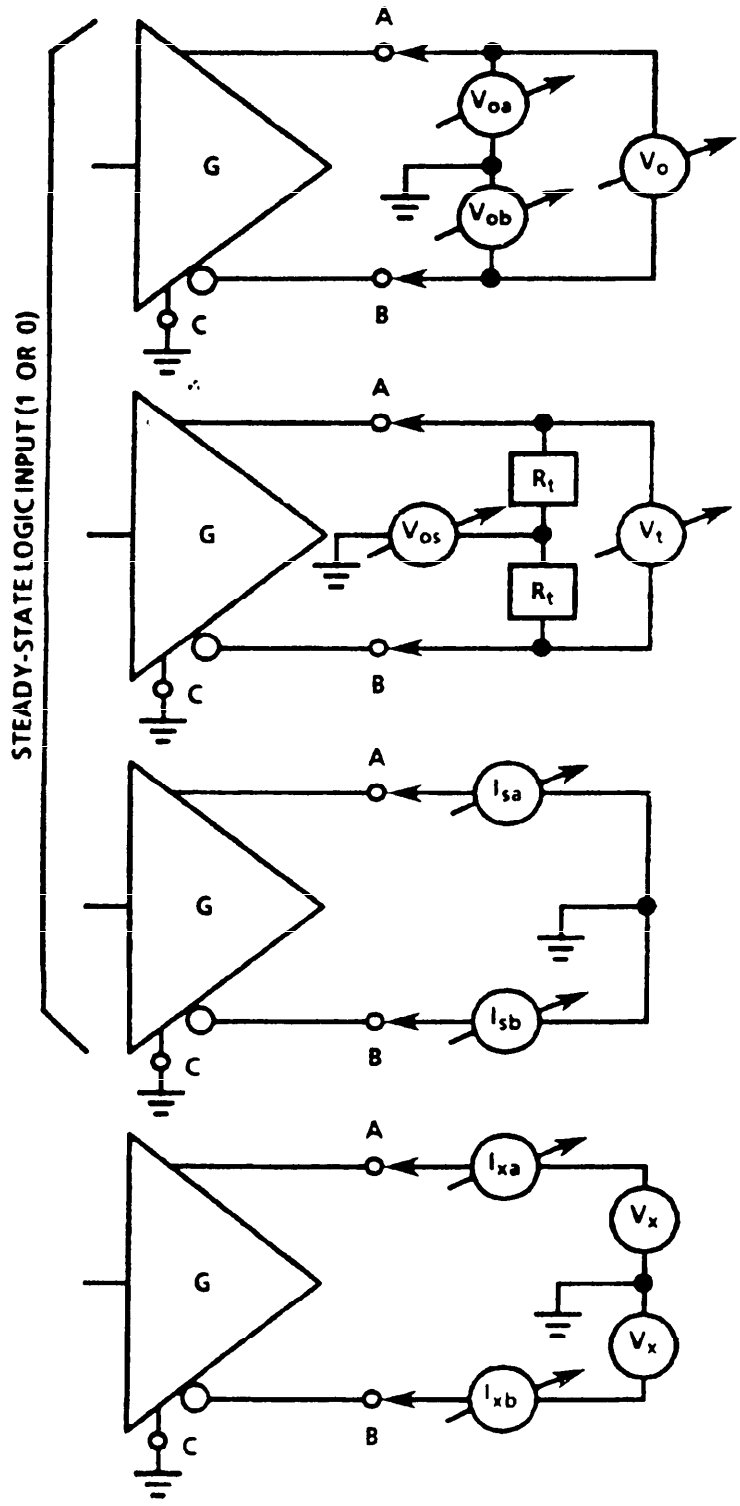
A', B' - LOAD INTERFACE POINTS

C' - LOAD CIRCUIT GROUND

R_t - OPTIONAL WIRE OR CABLE TERMINATION RESISTANCE

V_g - GROUND POTENTIAL DIFFERENCE

FIGURE 10. Balanced voltage digital interface circuit.



OPEN CIRCUIT MEASUREMENT
FOR EITHER BINARY STATE:
$4\ V \le |V_o| \le 6\ V$
TYPE I: $2\ V \le |V_{oa}| \le 3$
$2\ V \le |V_{ob}| \le 3$
TYPE II: $|V_{oa}| \le 6\ V$
$|V_{ob}| \le 6\ V$

TEST TERMINATION MEASUREMENT
FOR EITHER BINARY STATE:
$|V_t| \ge 0.5|V_o|$
$||V_t| - |\overline{V}_t|| \le 0.4\ V$
$|V_{os} - \overline{V}_{os}| \le 0.4\ V$
TYPE I: $|V_{os}| \le 0.4\ V$
TYPE II: $|V_{os}| \le 3\ V$

SHORT CIRCUIT MEASUREMENT
FOR EITHER BINARY STATE:
$|I_{sa}| \le 150\ mA$
$|I_{sb}| \le 150\ mA$

POWER-OFF MEASUREMENT
$|I_{xa}| \le 100\ \mu A$
$|I_{xb}| \le 100\ \mu A$
V_x IS APPLIED VOLTAGE
TYPE I: V_x FROM –6 V TO + 6V
TYPE II: V_x FROM –0.25 V TO + 6 V

FIGURE 11. Balanced generator parameter measurements.

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open-circuit voltages V_{oa} and V_{ob} measured between the generator output terminals A or B and the generator circuit ground (terminal C) shall not be more than 6 volts.

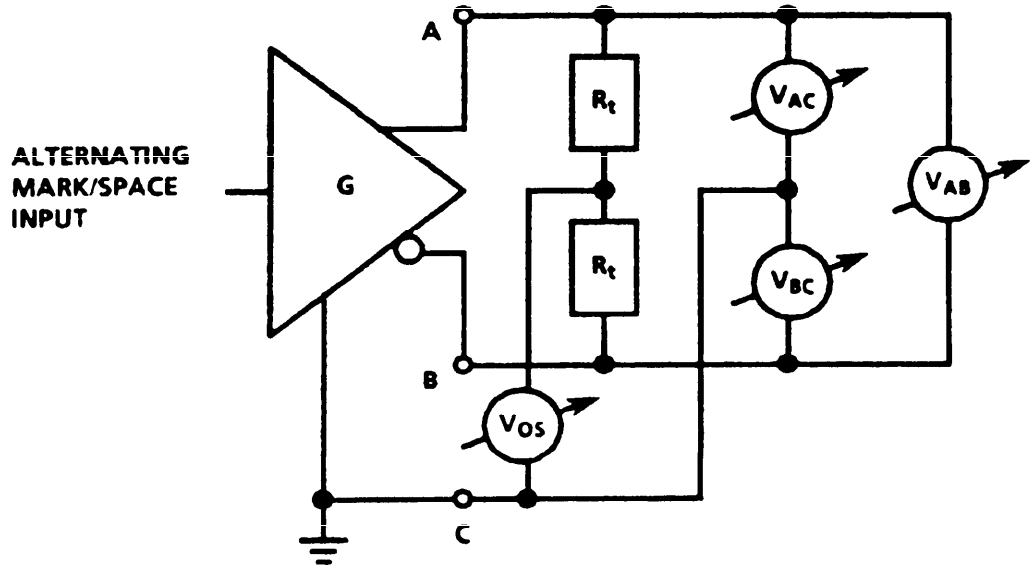
5.2.1.4 Test termination measurement. (See Figure 11.) With a test load of two resistors, 50 ohms ±1 percent each, connected in series between the generator output terminals A and B, the magnitude of the differential voltage V_t measured between the output terminals A and B shall not be less than one-half of the absolute value of V_o (see 5.2.1.3). For the opposite binary state the polarity of V_t shall be reversed (∇_t). The magnitude of the difference of the absolute values of V_t and ∇_t shall not be more than 0.4 volts. The magnitude of the difference of V_{os} for one binary state and ∇_{os} for the opposite binary state shall not be more than 0.4 volts. For type I generators (see 4.4.1), the magnitude of the generator offset voltage V_{os} measured between the center point of the test load and generator circuit ground (terminal C) shall not be more than 0.4 volts for either binary state. For type II generators (see 4.4.1), the magnitude of the generator offset voltage V_{os} shall not be more than 3 volts for either binary state.

NOTE: Nominal voltage waveforms for alternating binary states are shown in Figure 12 for type I and type II generators (see 4.4.1). These waveforms are intended to represent a typical balanced generator output signal, such as displayed on an oscilloscope.

5.2.1.5 Short-circuit measurement. (See Figure 12.) With the generator output terminals A and B short-circuited to generator circuit ground (terminal C), the magnitudes of the currents flowing through each generator output terminal shall not exceed 150 mA for either binary state.

5.2.1.6 Power-off measurement. (See Figure 12.) Under power-off conditions, the magnitude of the generator output leakage current I_{xa} and I_{xb} shall not exceed 100 microamperes with a voltage V_x applied between each generator output terminal A or B and generator circuit ground (terminal C). For type I generators (see 4.4.1) the terminal AC/BC voltages V_x shall range between +6 volts and -6 volts, and for type II generators the terminal AC/BC voltages V_x shall range between +6 volts and -0.25 volts.

5.2.1.7 Output signal waveform. (See Figure 13.) During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the differential signal measured across a 100 ohms ±10 percent test load connected between the generator output terminals A and B shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{ss} within 0.1 of the unit interval t_b or 20 nanoseconds (ns), whichever is greater. Thereafter, the signal voltage shall not vary more than 10 percent of V_{ss} from the steady state value, until the next binary transition occurs, and at no time



LEGEND: R_t = 50 ohms

TYPE I GENERATOR

ASSUMPTION: $|V_{AB}| = 5$ V

$|V_{OS}| = 0$ V

TYPE II GENERATOR

ASSUMPTION: $|V_{AB}| = 5$ V

$|V_{OS}| = 2.5$ V

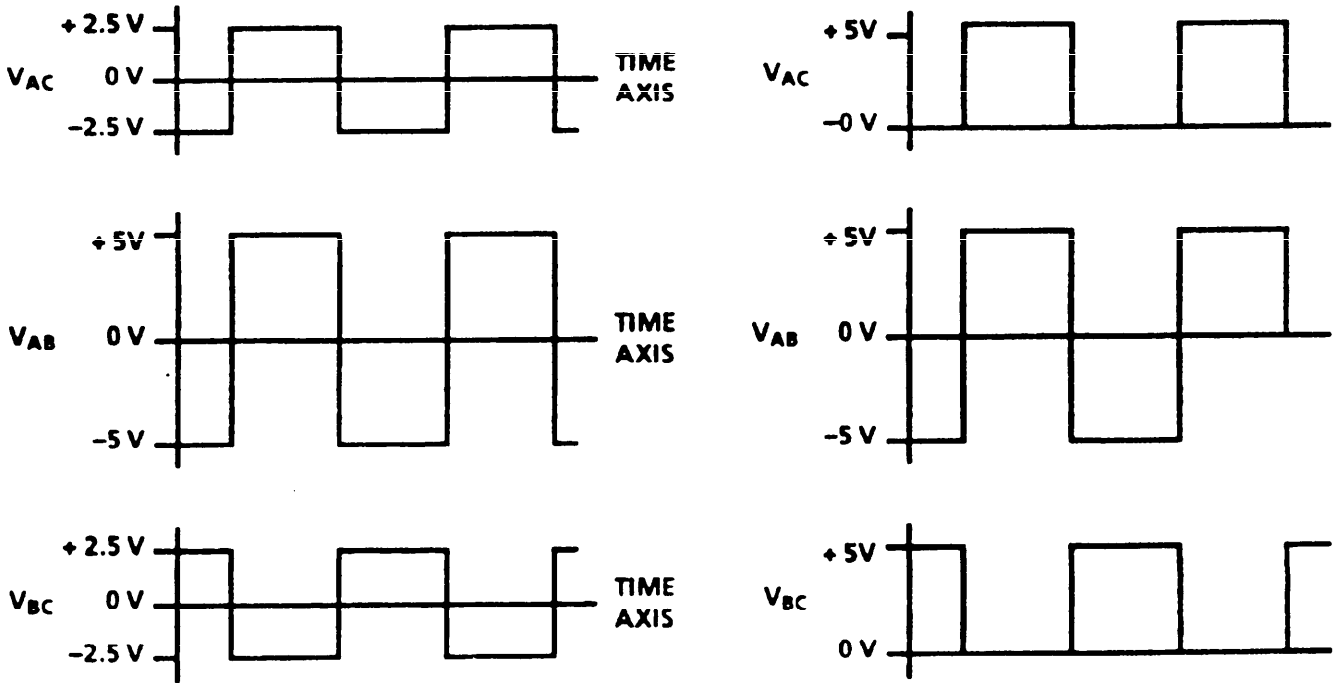
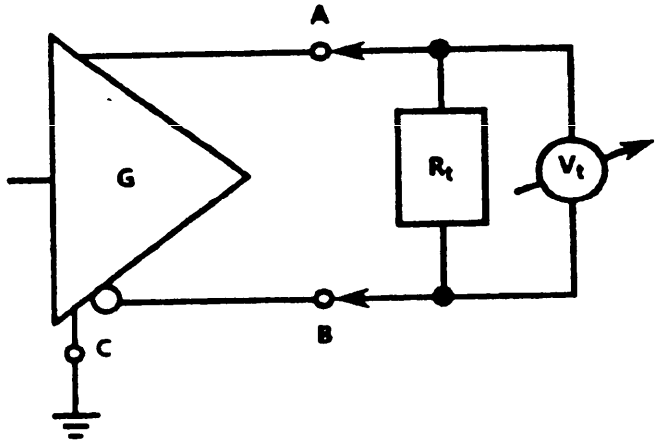
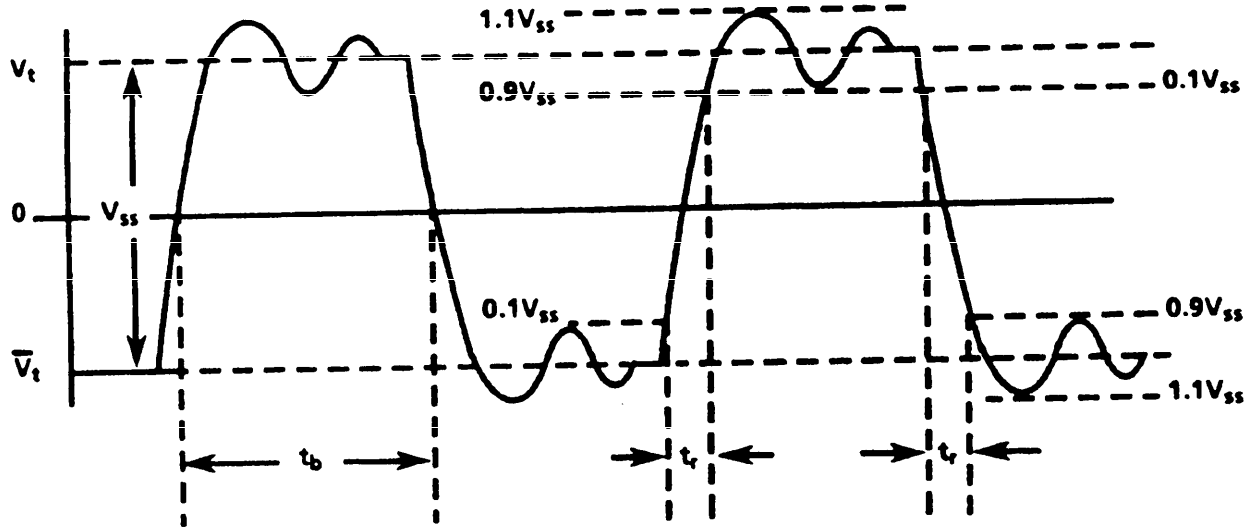


FIGURE 12. Nominal waveforms of type I and type II generators.





LEGEND: R_t = 100 ohms, ± 10 PERCENT
$|V_{ss}|$ = $|V_t - \overline{V}_t|$
V_{ss} = DIFFERENCE IN STEADY STATE VOLTAGES
t_b = UNIT INTERVAL
t_r = RISETIME
t_r ≤ 0.1 t_b OR 20 ns, WHICHEVER IS GREATER

FIGURE 13. Balanced generator output signal waveform.

shall the instantaneous magnitude of V_t or ∇_t exceed 6 volts, nor be less than 2 volts. V_{ss} is defined as the voltage difference between the two terminated steady state values (V_t and ∇_t) of the generator output.

NOTE: The lower limit of the risetime t_r is not standardized. The upper limit of the risetime t_r is either 0.1 of the unit interval t_b or 20 ns, whichever is greater.

5.2.1.8 High impedance output state. The generator output should be permitted to assume a high impedance state, if required for multiple generator bus operation. If a high impedance state is implemented, the output voltage shall be nominally zero for the high impedance state when measured with a test termination as stated in 5.2.1.4.

5.2.2 Wire or cable characteristics. Not standardized.

Note: Guidelines on wire or cable characteristics are given in 30.3 of Appendix C.

5.2.3 Load characteristics. The load consists of one or more receivers (R) and an optional wire or cable termination resistance (R_t) as shown in Figure 10. Guidelines on the need for a wire or cable termination resistance are given in 30.4 of Appendix C. The electrical characteristics of a single receiver without optional wire or cable termination and fail safe provision are specified in terms of the measurements illustrated in Figures 7 through 9 and described in 5.1.3.1 through 5.1.3.3. A device meeting these requirements results in a differential receiver having a high input impedance (4000 ohms or more), a small input threshold transition region between -0.2 volts and +0.2 volts, and allowance for an internal bias voltage not to exceed 3 volts in magnitude. Multiple receivers and a provision for fail safe operation for specific applications are allowed in the load within the limitations specified in 5.2.3.6. The receiver used in the load for the balanced voltage digital interface circuit is electrically identical to the receiver for the unbalanced voltage digital interface circuit stated in 5.1 and for the terminated voltage digital interface circuit stated in 5.3.

5.2.3.1 Receiver input current-voltage measurement. Same as 5.1.3.1.

5.2.3.2 Receiver input sensitivity measurement. Same as 5.1.3.2.

5.2.3.3 Receiver input balance measurement. Same as 5.1.3.3.

5.2.3.4 Multiple receivers. Not standardized.

NOTE: The use of up to ten receivers in the load may be optionally employed. Extreme caution must be exercised to avoid performance degradation due to signal reflections from stub lines emanating from the load interface point to the receivers. See 5.2.3.6 for limits on total load resistance and sensitivity.

5.2.3.5 Fail-safe operation. Where a fail-safe is required, a provision shall be incorporated in the load to provide a steady binary condition (either MARK or SPACE as required by the application) to protect against certain fault conditions.

NOTE: The method of providing fail-safe is not standardized. An example of fail-safe operation is given in 30.5.2 of Appendix C.

5.2.3.6 Total load characteristic limits. The total load, including multiple receivers, fail-safe provisions, and wire or cable termination (if implemented), shall have a resistance greater than 120 ohms between its input points (terminals A' and B' of Figure 10) and shall require a differential input voltage of not more than 200 mV for all receivers to assume the intended binary state.

5.2.3.7 Wire or cable termination resistance. Not standardized.

NOTE: The use of a wire or cable termination resistance (R_t) is optional, depending upon the specific environment in which the interface circuit is employed. See 5.2.3.6 for limits on total load resistance and 30.4 of Appendix C for guidelines on the need for a wire or cable termination resistance.

5.2.4 Operational constraints. A balanced voltage digital interface circuit conforming to 5.2 will perform satisfactorily at signaling rates up to 10 Mb/s providing that the following operational constraints are simultaneously satisfied:

a. The interconnecting wire or cable length is within that recommended for the applicable signaling rate indicated in 30.3.6 of Appendix C, and the wire or cable is appropriately terminated.

b. The common mode voltage at the receiver is less than 7 volts (peak). The common mode voltage is defined to be any uncompensated combination of generator-receiver ground potential difference, the generator offset voltage V_{os}, and longitudinally coupled peak random noise voltage measured between the receiver circuit ground and the wire or cable with the generator ends of the wire or cable short-circuited to ground.

NOTE 1: The use of type II generators with up to 3 volts of offset voltage will reduce the common mode noise protection margin by an amount proportional to the value of the offset voltage.

NOTE 2: Care should be taken when power for distant receivers is supplied in the same or in adjacent conductors as used for data, clock or control signals, in order to avoid performance degradation that may be caused by power supply surges and spurious voltage transients.

5.2.5 Circuit protection. Same as 5.1.5.

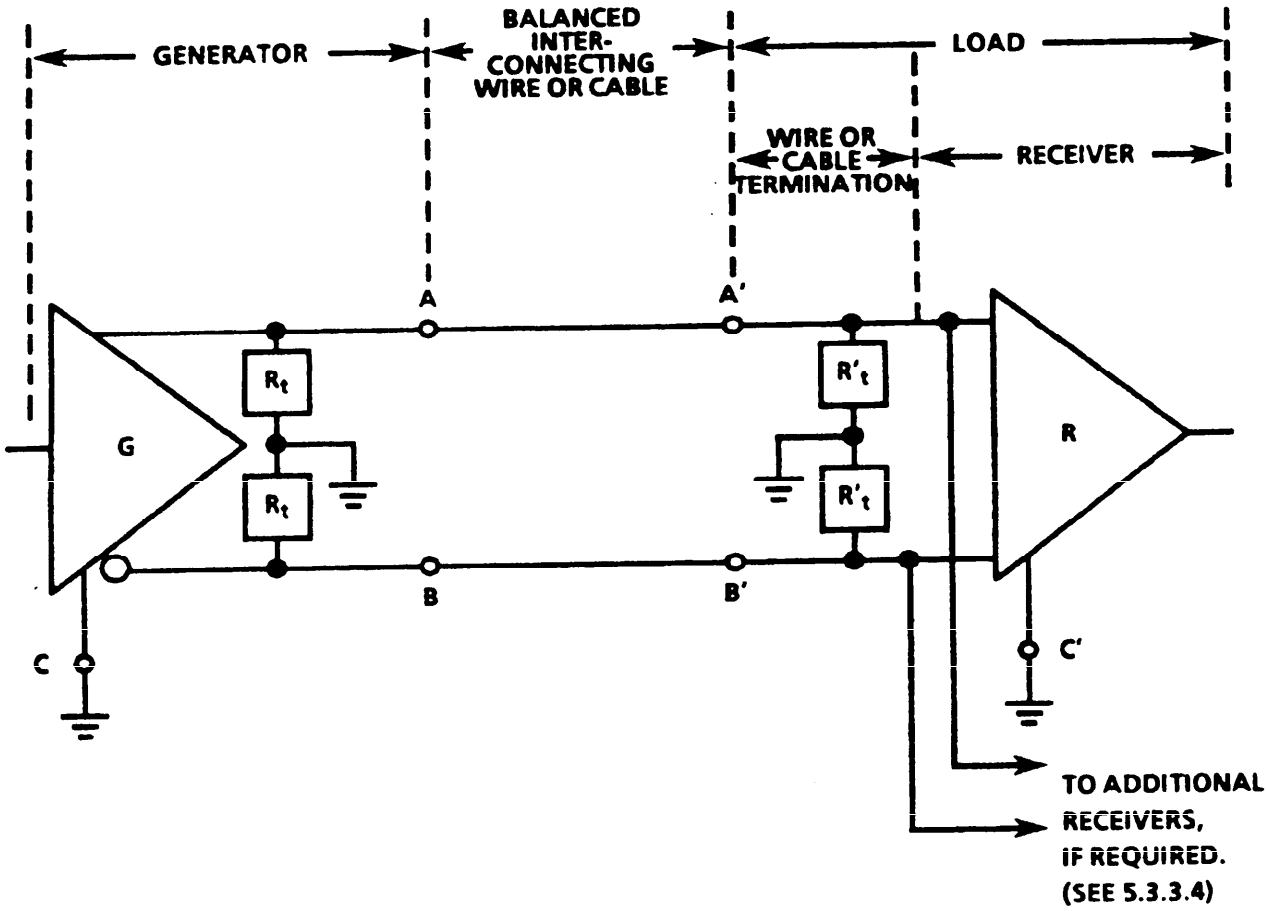
5.3 Terminated voltage digital interface circuit. The terminated voltage digital interface circuit is a balanced voltage circuit and is shown in Figure 14. The circuit consists of three parts: the terminated voltage generator (G) which is a type III generator (see 4.4.1), the balanced interconnecting wire or cable, and the load. The terminated voltage generator requires a termination resistance (R_t), with a grounded center tap. The termination resistance (R_t), although external to the generator, is considered to be part of the generator circuit and is necessary to match the relatively high generator source impedance to the characteristic impedance of the transmission line. A similar type termination is also required at the end of the transmission line where the receiver is connected. The terminated voltage generator has characteristics similar to, and may be treated like, a constant-current generator, although the actual implementation may not be a true constant-current generator. It should be noted that the use of a termination at the constant-current generator output actually causes a voltage waveform to be generated which in turn drives the transmission line. The voltage polarity reverses when the current direction changes. The advantage of this circuit configuration is that the rise and fall time of the voltage waveform is primarily determined by the constant-current generator and is relatively unaffected by the transmission line characteristics, which is important for signaling rates above 10 Mb/s. The load consists of one or more receivers (R), (see 5.3.3.4) and a wire or cable termination resistance (R_t'). The termination resistance (R_t') is selected to match the characteristic impedance of the transmission line to the relatively high input impedance of the receiver.

5.3.1 Generator characteristics. The electrical characteristics of the type III generator (see 4.4.1) are specified in accordance with the measurements illustrated in Figures 15 and 16 and described in 5.3.1.1 through 5.3.1.7. The measurements are under static conditions, whereas measurements under dynamic conditions are not standardized. A generator meeting these requirements results in a low impedance (150 ohms or less) balanced voltage source that will produce a differential voltage applied to the interconnecting wire or cable in the range of 2 volts to 6 volts.

5.3.1.1 Signal sense. The signal sense of the generator output voltages appearing across the interconnecting wire or cable (see Figure 14) shall be as shown in Table II. (See Note of 5.1.1.1.)

5.3.1.2 Signaling rate range. Not standardized. (See 4.3.)

5.3.1.3 Output voltage measurement. (See Figure 15.) With a termination of two resistors (R_t), each between 50 ohms and 75 ohms, connected in series between the generator output terminals A and B and balanced to ground within ±1 percent, the magnitude of the differential voltage (V_t) measured between the generator output terminals A and B shall not be less than 2 volts nor



LEGEND:

R_t, R'_t - TERMINATION RESISTANCE
A, B - GENERATOR INTERFACE POINTS
A', B' - LOAD INTERFACE POINTS
C - GENERATOR CIRCUIT GROUND
C' - LOAD CIRCUIT GROUND

FIGURE 14. Terminated voltage digital interface circuit.

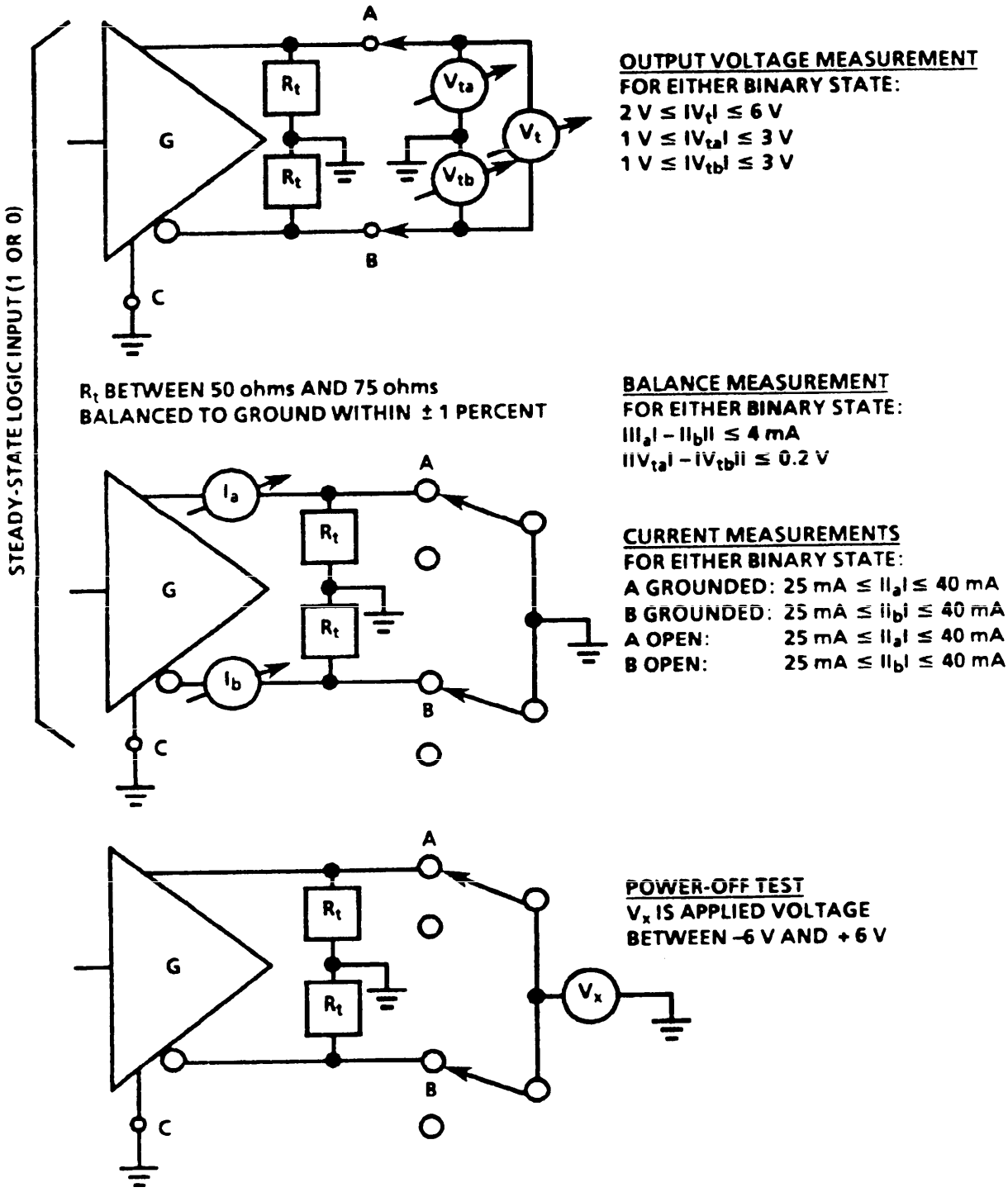


FIGURE 15. Terminated voltage generator parameter measurements.

more than 6 volts for either binary state. The magnitudes of V_{ta} and V_{tb} measured between the generator output terminals A or B and the generator circuit ground (terminal C) shall not be less than 1 volt nor more than 3 volts.

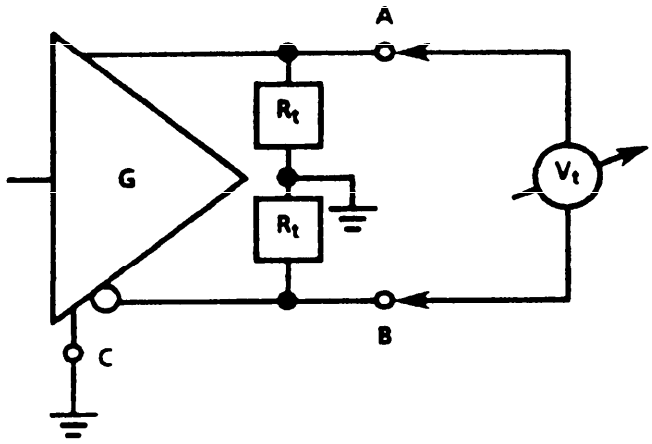
5.3.1.4 Balance measurement. (See Figure 15.) With a termination of two resistors (R_t), each between 50 ohms and 75 ohms, connected in series between the generator output terminals A and B and balanced to ground within ±1 percent, the magnitude of the difference of the absolute values of I_a and I_b shall be less than or equal to 4 mA. The current balance shall be verified by measuring the voltage drops V_{ta} and V_{tb}. The magnitude of the difference of the absolute values of V_{ta} and V_{tb} shall be less than or equal to 0.2 volts, for either binary state.

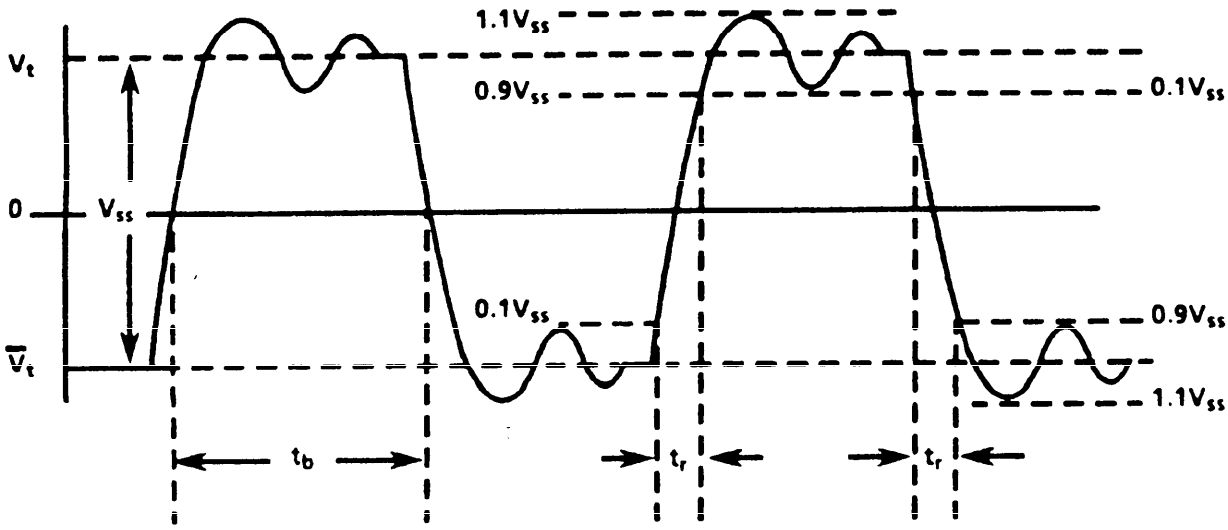
5.3.1.5 Current measurements. (See Figure 15.) With the generator output terminal A or B, or both, short-circuited (grounded) to generator circuit ground (terminal C) or open (ungrounded), the magnitudes of the currents I_a and I_b flowing through each generator output terminal shall not be less than 25 mA nor more than 40 mA for either binary state. The magnitude of the difference of the absolute values of the grounded and ungrounded (open) generator currents I_a and I_b shall be less than or equal to 4 mA for either binary state.

5.3.1.6 Power-off test. (See Figure 15.) Under power-off conditions, the generator shall not be damaged by an external voltage V_x ranging between +6 volts and -6 volts applied between either or both output terminals A and B and generator circuit ground (terminal C).

5.3.1.7 Output signal waveform. (See Figure 16.) During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the differential signal measured across a termination of two resistors (R_t), each between 50 ohms and 75 ohms, connected in series between generator output terminals A and B and generator circuit ground and balanced to ground within ±1 percent, shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{ss} within 5 ns when the unit interval t_b is less than or equal to 20 ns. When the unit interval t_b is between 20 ns and 50 ns, the differential signal shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{ss} within 12 ns. Thereafter, the signal voltage shall not vary more than 10 percent of V_{ss} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of V_t or $\overline{V}_t$ exceed 6 volts, nor be less than 2 volts. V_{ss} is defined as the voltage difference between the two steady state values (V_t and $\overline{V}_t$) of the generator output.

NOTE: The lower limit of the risetime t_r is not standardized.





LEGEND: t_b = UNIT INTERVAL
t_r = RISETIME
t_r ≤ 12 ns WHEN 20 ns < t_b < 50 ns
t_r ≤ 5 ns WHEN t_b ≤ 20 ns
V_{ss} = DIFFERENCE IN STEADY STATE VOLTAGES
$|V_{ss}| = |V_t - \overline{V_t}|$
R_t = SEE 5.3.1.7

FIGURE 16. Terminated voltage generator output signal waveform.

5.3.2 Wire or cable characteristics. (See Figure 14.) The interconnecting wire or cable shall be balanced to ground and shall have a characteristic impedance between 100 ohms and 150 ohms measured at 10 megahertz (MHz).

5.3.3 Load characteristics. (See Figure 14.) The load consists of one or more receivers (R) and a balanced termination resistance (R_t') which is identical to the generator termination. The receiver is the same as the receiver of the unbalanced and balanced voltage digital interface circuits stated in 5.1.3 and 5.2.3, respectively, with the exceptions of the requirements for multiple receivers (see 5.3.3.4), total load characteristic limits (see 5.3.3.6) and wire or cable termination resistance (see 5.3.3.7).

5.3.3.1 Receiver input current-voltage measurement. Same as 5.1.3.1.

5.3.3.2 Receiver input sensitivity measurement. Same as 5.1.3.2.

5.3.3.3 Receiver input balance measurement. Same as 5.1.3.3.

5.3.3.4 Multiple receivers. (See Figure 14.) No more than two monitor circuits or additional receivers shall be employed. The monitor circuits or additional receivers shall have an input impedance greater than or equal to 4000 ohms. To avoid reflections, care should be exercised to keep the stub lines emanating from the load interface point to the receivers or monitors to less than 3 meters in length.

5.3.3.5 Fail-safe operation. Same as 5.2.3.5.

5.3.3.6 Total load characteristic limits. The total load including multiple receivers, fail-safe provisions, and wire or cable termination shall have a resistance greater than 95 ohms between its input points (terminals A' and B' of Figure 14) and shall require a differential input voltage of not more than 200 mV for all receivers to assume the intended binary state.

5.3.3.7 Wire or cable termination resistance. (See Figure 14). The wire or cable termination shall consist of two resistors connected in series, equal in value to those used as a generator termination (see 5.3.1), and balanced to ground within ±1 percent.

5.3.4 Operational constraints. Under consideration.

5.3.5 Circuit protection. Same as 5.1.5.

5.4 Functional interchange circuits. Functional interchange circuits are described in 4.2 and shown as an example in Figure 17.

5.4.1 Interchange circuit requirements. For the exchange of information between DTE and DCE, the functional interchange circuits listed in Table III, or an applicable subset, shall be used. A receive-only asynchronous balanced interface, for example, shall use the receive data and signal ground circuits, as a minimum configuration. The signal ground interchange circuit

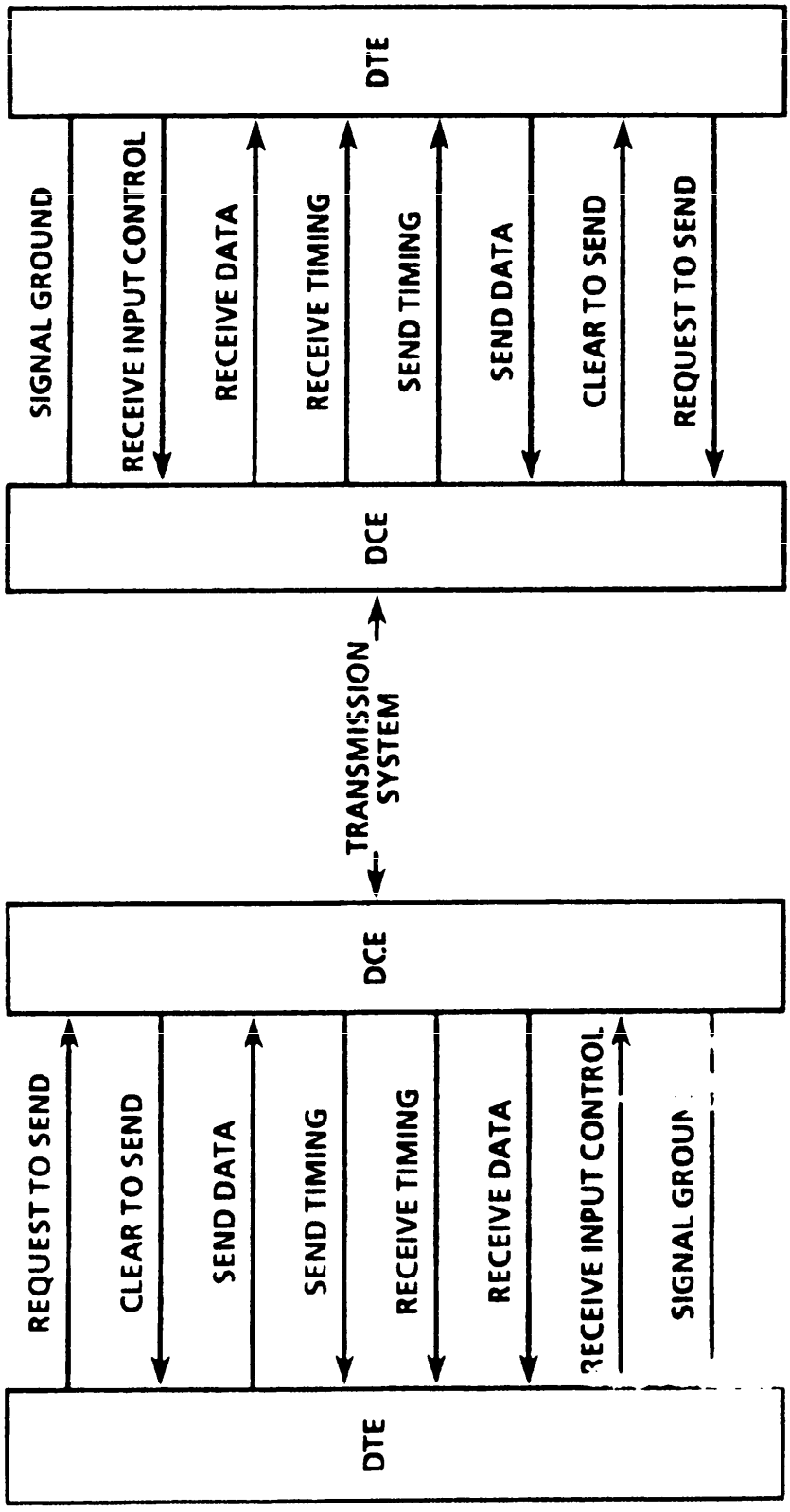


FIGURE 17. Example of functional interchange circuits.

shall be used in all interfaces. The send common and receive common shall be used as shared returns in each signal direction, as required, for unbalanced circuits not having individual separate returns.

TABLE III. Functional interchange circuits.

CIRCUIT	DIRECTION
REQUEST TO SEND	FROM DTE TO DCE
CLEAR TO SEND	FROM DCE TO DTE
RECEIVE INPUT CONTROL	FROM DTE TO DCE
SEND DATA	FROM DTE TO DCE
RECEIVE DATA	FROM DCE TO DTE
SEND TIMING	FROM DCE TO DTE
RECEIVE TIMING	FROM DCE TO DTE
SEND COMMON	RETURN
RECEIVE COMMON	RETURN
SIGNAL GROUND	GROUND

5.4.2 Interchange circuit functions. The interchange circuits listed in Table III shall function as stated in 5.4.2.1 through 5.4.2.10.

5.4.2.1 Request to send. This circuit shall control the data channel transmit function of the DCE and shall control the direction of data transmission of the DCE on a half-duplex channel. On one way only or duplex channels, the ON signal sense (see Table II) shall maintain the DCE in the transmit mode, and the OFF signal sense shall maintain the DCE in a non-transmit mode. On a half-duplex channel, the ON signal sense shall maintain the DCE in the transmit mode and shall inhibit the receive mode, and the OFF signal sense shall maintain the DCE in the receive mode.

5.4.2.2 Clear to send. This circuit shall be used to indicate to the DTE that the DCE is ready to transmit data on the data channel. The ON signal sense (see Table II) shall indicate that the DCE is ready to transmit data, and the OFF signal sense shall indicate that the DCE is not ready to transmit data.

5.4.2.3 Receive input control. This circuit shall be used to indicate to the DCE that the DTE is ready to receive data. The ON signal sense (see Table II) shall indicate that the DTE is ready to receive data, and the OFF signal sense shall indicate that the DTE is not ready to receive data.

5.4.2.4 Send data. This circuit shall be used to transmit data from the DTE to the DCE. The DTE shall not transmit data unless its clear to send circuit is receiving the ON signal sense. (See Table II.)

5.4.2.5 Receive data. This circuit shall be used to transmit data from the DCE to the DTE.

5.4.2.6 Send timing. This circuit shall be used to provide the DTE with transmit signal element timing information.

NOTE: Detailed requirements for clock equipment, control and timing are contained in subparagraph 4.3.1.6 of MIL-STD-188-100 and subparagraph 5.3.6 of MIL-STD-188-200.

5.4.2.7 Receive timing. This circuit shall be used to provide the DTE with receive signal element timing information. (See Note of 5.4.2.6.)

5.4.2.8 Send common. This circuit shall be connected to the DTE circuit ground (circuit common) and shall be used at the DCE as a reference potential for the receiver(s) of the unbalanced voltage digital interface circuit when separate signal returns are not used. (See Figure 24 of Appendix C.)

5.4.2.9 Receive common. This circuit shall be connected to the DCE circuit ground (circuit common) and shall be used at the DTE as a reference potential for the receiver of the unbalanced voltage digital interface circuit when separate signal returns are not used. (See Figure 24 of Appendix C.)

5.4.2.10 Signal ground. This circuit shall connect the DTE circuit ground (circuit common) to the DCE circuit ground (circuit common) to provide a metallic path between the DTE and DCE signal commons.

Custodians:

Army - CR
Navy - EC
Air Force - 17

Preparing activity:

Army - CR
(Project TCTS - 1141)

Review activities:

Army - AC, AV, MI, SC, TE
Navy - AS, CG, MC, NC, OM, SA, SH, YD
Air Force - 01, 11, 13, 71, 80
DCA - DC
NSA - NS
JTC^{3}A - C^3

User activites

Army
Navy
Air Force

International interest:

ABCA

Other Interests:

DODECAC
NCS

APPENDIX A

MEMORANDUM FROM THE UNDER SECRETARY OF DEFENSE FOR RESEARCH AND ENGINEERING, 16 AUGUST 1983, SUBJECT: MANDATORY USE OF MILITARY TELECOMMUNICATIONS STANDARDS IN THE MIL-STD-188 SERIES

This Appendix contains information related to MIL-STD-188-114A. Appendix A is a mandatory part of this standard.

THE UNDER SECRETARY OF DEFENSE
WASHINGTON, D.C. 20301

RESEARCH AND ENGINEERING

16 AUG 1983

MEMORANDUM FOR ASSISTANT SECRETARY OF THE ARMY (INSTALLATIONS, LOGISTICS & FINANCIAL MANAGEMENT)
ASSISTANT SECRETARY OF THE NAVY (SHIPBUILDING & LOGISTICS)
ASSISTANT SECRETARY OF THE AIR FORCE (RESEARCH DEVELOPMENT & LOGISTICS)
COMMANDANT OF THE MARINE CORPS
DIRECTOR, DEFENSE COMMUNICATIONS AGENCY
DIRECTOR, NATIONAL SECURITY AGENCY

SUBJECT: Mandatory Use of Military Telecommunications Standards in the MIL-STD-188 Series

On May 10, 1977, Dr. Gerald Dinneen, then Assistant Secretary of Defense(C^3I), issued the following policy statement regarding the mandatory nature of the MIL-STD-188 series telecommunications standards:

"...standards as a general rule are now cited as 'approved for use' rather than 'mandatory for use' in the Department of Defense.

This deference to the judgment of the designing and procuring agencies is clearly appropriate to standards dealing with process, component ruggedness and reliability, paint finishes, and the like. It is clearly not appropriate to standards such as those in the MIL-STD-188 series which address telecommunication design parameters. These influence the functional integrity of telecommunication systems and their ability to efficiently interoperate with other functionally similar Government and commercial systems. Therefore, relevant military standards in the 188 series will continue to be mandatory for use within the Department of Defense.

To minimize the probability of misapplication of these standards, it is incumbent upon the developers of the MIL-STD-188 series to insure that each standard is not only essential but of uniformly high quality, clear and concise as to application, and wherever possible compatible with existing or proposed national, international and Federal telecommunication standards. It is also incumbent upon the users of these standards to cite in their procurement specifications only those standards which are clearly necessary to the proper functioning of the device or systems over its projected lifetime."

This statement has been reviewed by this office and continues to be the policy of the Department of Defense.

APPENDIX B
ABBREVIATIONS AND ACRONYMS

20. GENERAL

20.1 Scope. The Appendix contains a list of abbreviations and acronyms used in MIL-STD-188-114A.

20.2 Application. This appendix is a non-mandatory part of MIL-STD-188-114A.

ABCA	American-British-Canadian-Australian
AWG	American wire gauge
bit	binary digit
b/s	bit(s) per second
CCITT	International Telegraph and Telephone Consultative Committee
dB	decibel
dc	direct current
DCE	data circuit terminating equipment
DTE	data terminal equipment
EIA	Electronics Industries Association
FED-STD	Federal standard
GHz	gigahertz (1 GHz = 10^9 hertz)
GWG	green wire ground
IC	integrated circuit
kb/s	kilobit(s) per second (1 kilobit = 1000 bits)
kHz	kilohertz (1 kHz = 1000 hertz)
km	kilometer
m	meter (s)

mA	milliampere
Mb/s	megabit(s) per second (1 Mb/s = 1,000,000 bits per second)
MHz	megahertz (1 MHz = 10^6 hertz)
MIL-STD	military standard
ms	millisecond(s) (1 ms = 10^{-3} seconds)
mV	millivolt(s) (1 mV = 10^{-31} volts)
ns	nanosecond(s) (1 ns = 10^{-9} seconds)
pF	picofarad (1 pF = 10^{-12} farad)
QSTAG	Quadripartite Standardization Agreement
RC	receive common
SC	send common
V	volt(s)

APPENDIX C
GUIDELINES ON INTERCONNECTIONS

30. GENERAL

30.1 Scope. This Appendix contains guidelines on the characteristics of the interconnecting wire or cable (30.3), on the need for providing a termination resistance (30.4), on fail safe operation (30.5), and on optional grounding arrangements (30.6). This appendix is not a mandatory part of MIL-STD-188-114A. The information contained herein is intended for guidance only.

30.2 Application. When interconnecting equipment using the electrical characteristics specified in this document, certain consideration should be given to some of the problems that may be encountered due to the interconnecting wire or cable characteristics, wire or cable termination resistance, and optional grounding arrangements.

30.3 Guidelines on interconnecting wire or cable characteristics. Guidelines on the characteristics of the interconnecting wire or cable are given in 30.3.1 through 30.3.6. An interconnecting wire or cable meeting these characteristics will result in a transmission line with a nominal characteristic impedance on the order of 100 ohms for frequencies greater than 100 kHz, and a dc series loop resistance not exceeding 240 ohms.

For the unbalanced voltage digital interface circuit, the wire or cable may be composed of twisted pair, or unpaired wires possessing the characteristics described in 30.3.1 through 30.3.3 uniformly over its lengths. Where twisted pair wire or cable is used and the two wires serve as signal conductors for two different interface circuits, the information flow in both wires should be in the same direction. The use of twisted pairs is preferred over the use of untwisted pairs to reduce crosstalk.

For the balanced voltage digital interface circuit, the wire or cable may be composed of twisted pair possessing the characteristics described in 30.3.1 through 30.3.4 uniformly over its length.

Most commonly available wire or cable used for telephone applications should meet the characteristics given in 30.3.1 through 30.3.4. The characteristics of standard field wire, such as WD-1 or WF-16, are considered sufficiently close to those characteristics given in the following subparagraphs as guidance, that these types of field wire may be used satisfactorily for unbalanced and balanced voltage digital interface circuits standardized in 5.1, 5.2 and 5.3.

30.3.1 Conductor size. The interconnecting wire or cable should be composed of wires of a 24 American wire gauge (AWG) or larger conductor for solid or stranded copper wires, or for non-copper conductors, a sufficient size to yield a dc wire resistance not to exceed 90 ohms per 1000 meters (m) (approximately 30 ohms per 1000 feet) per conductor.

30.3.2 Mutual pair capacitance. For paired wires, the capacitance between one wire in the pair to the other wire should not exceed 60 picofarads per meter (approximately 20 picofarads per foot), and the value should be reasonably uniform over the length of the wire or cable.

30.3.3 Stray capacitance. The capacitance between one wire in the cable to all other wires in the cable sheath, with all other wires connected to ground, should not exceed 120 picofarads per meter (approximately 40 picofarads per foot) and the value should be reasonably uniform for a given conductor over the length of the wire or cable.

30.3.4 Pair-to-pair balanced crosstalk. For balanced voltage digital interface circuits, the balanced crosstalk from one pair of wires to any other pair in the same cable sheath should have a minimum value of 40 dB of attenuation measured at 150 kHz.

30.3.5 Wire or cable length for unbalanced voltage digital interface circuit. The maximum operating distance is primarily a function of the amount of interference (near-end crosstalk) coupled to adjacent circuits in the equipment interconnection. Additionally, the unbalanced circuit is susceptible to exposure to differential noise resulting from any imbalance between the signal conductor and signal common return at the load interface point. Increasing the physical separation and interconnecting wire or cable length between the generator and load interface points increases the exposure to common mode noise and the amount of near-end crosstalk. Accordingly, users are advised to restrict the wire or cable length to a minimum, consistent with the requirements for physical separation between generator and load.

The curve of signaling rate or cable length versus risetime given in Figure 18 may be used as a conservative guide. This curve is based upon calculations and empirical data using twisted pair telephone cable with a shunt capacitance of 50 picofarads per meter (approximately 16 picofarads per foot), a 50-ohm generator impedance, a 12-volt peak-to-peak generator signal, and allowing a maximum near-end crosstalk of 1 volt peak. The rise time (t_r) of the generator signal at signaling rates below 1 kb/s is 100 microseconds and above 1 kb/s is 0.1 unit interval (see 5.1.1.8).

The user is cautioned that the curve given in Figure 18 does not account for common mode noise or near-end crosstalk levels beyond the limits specified that may be introduced between the generator and load by exceptionally long cables. On the other hand, while signal quality degradation within the bounds of Figure 18 will ensure a zero-voltage crossing ambiguity of less than 0.05 unit interval, many applications can tolerate greater timing and amplitude distortion. Thus, correspondingly greater cable lengths may be employed than those indicated. The generation of near-end crosstalk can be reduced by using a lower generator resistance and increasing the amount of waveshaping employed. In practice, the maximum length of the wire or cable that may be used must be determined on a case by case basis. Experience has shown in most practical cases that the operating distance at lower signaling rates may be extended to several miles.

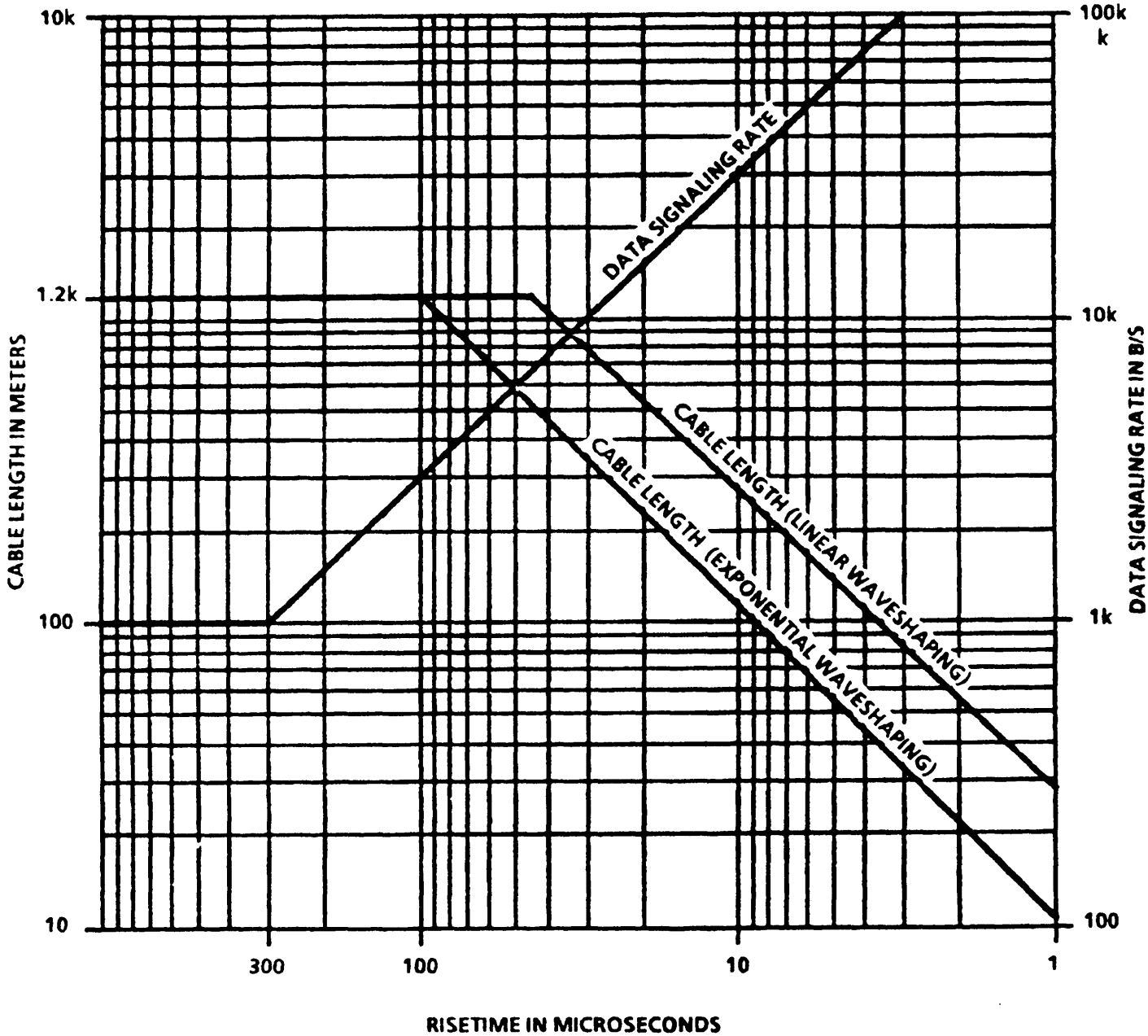


FIGURE 18. Signaling rate or cable length versus risetime for unbalanced voltage digital interface circuit.

In selecting wire or cable for a given application, the resistance and capacitance per unit length should be considered. Figure 19 shows the cable RC time constant versus cable length for cable pairs with different characteristics. As long as the signal rise time allows the signal to achieve full amplitude within the unit interval, cable capacitance normally will not be a problem. Conservative design would limit the rise time to less than 30 percent of the unit interval.

30.3.6 Wire or cable length for balanced voltage digital interface circuit. The maximum permissible length of wire or cable separating the generator and load is a function of signaling rate and is influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and ground potential difference introduced between the generator and load circuit grounds, as well as by wire or cable balance. Increasing the physical separation and interconnecting wire or cable length between the generator and load interface points, increases the exposure to common mode noise, signal distortion, and the effects of wire or cable imbalance. Accordingly, users are advised to restrict wire or cable length to a minimum, consistent with the requirements for physical separation between generator and load.

The curve of signaling rate versus cable length given in Figure 20 may be used as a conservative guide. This curve is based upon empirical data using a 24 AWG twisted-pair telephone cable terminated in a 100-ohm resistive load. The cable length restriction shown by the curve is based upon assumed load signal quality requirements of:

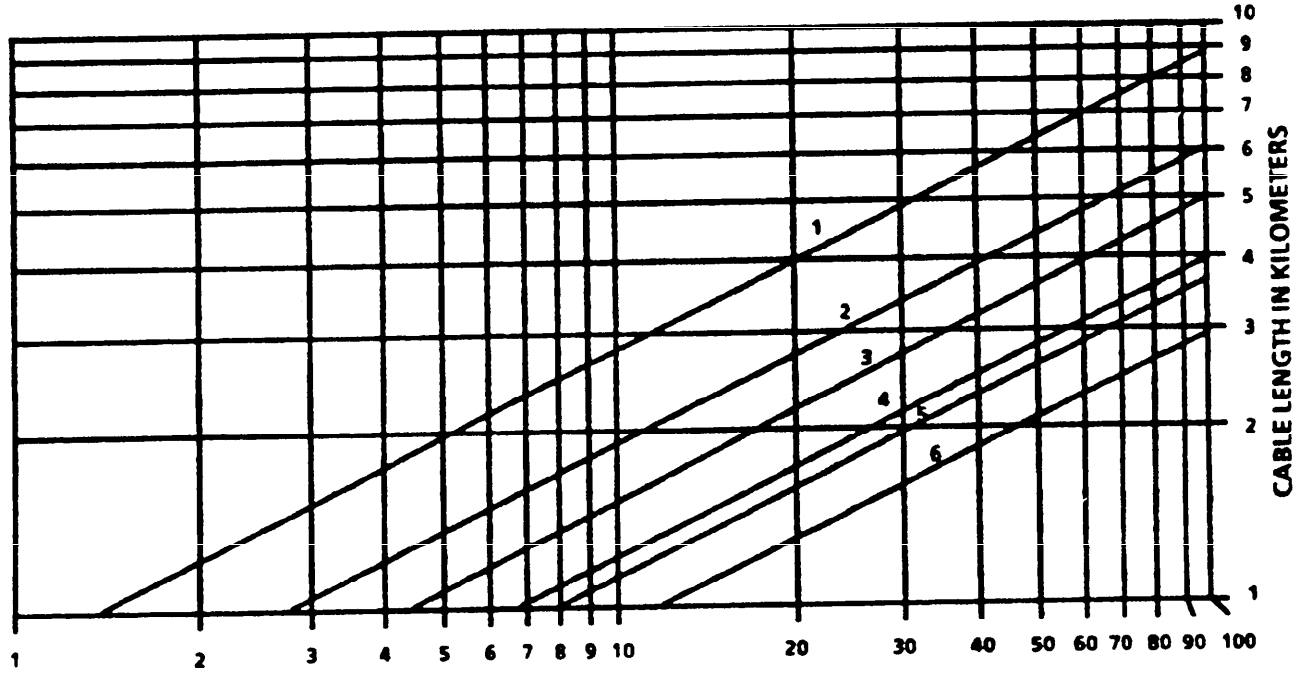
a. Signal rise and fall time equal to, or less than one-half unit interval at the applicable signaling rate.

b. A maximum voltage loss between generator and load of 6 dB.

Neglecting noise, interfaces can actually tolerate much greater voltage losses. For example, using a generator with an output voltage of 4 volts and a receiver with a sensitivity of 0.2 volts, allows a 20 to 1 voltage loss or 26 dB of attenuation. However, any noise present on the cable may cause additional zero-voltage crossings of the signal and an increase of the bit error rate.

At the higher signaling rates (90 kb/s to 10 Mb/s) the sloping portion of the curve in Figure 20 shows the cable length limitation established by the assumed signal rise time requirements. As the signaling rate is reduced below 90 kb/s, the cable length has been limited at 1200 meters (approximately 4000 feet) by the assumed maximum allowable 6 dB signal voltage loss.

The user is cautioned that the curve given in Figure 20 does not account for cable imbalance, or common mode noise beyond the limits specified that may be introduced between the generator and load by exceptionally long cables. On the other hand, while signal quality degradation within the bounds of Figure 20 will ensure a zero-voltage crossing ambiguity of less



CABLE TYPES:
1. AWG 19 (27 ohms/km, 50 pF/m)
2. AWG 22 (54 ohms/km, 50 pF/m)
3. AWG 24 (82 ohms/km, 50 pF/m)
4. AWG 26 (134 ohms/km, 50 pF/m)
5. AWG 22 (54 ohms/km, 150 pF/m)
6. AWG 24 (82 ohms/km, 150 pF/m)

FIGURE 19. Cable pair RC time constant versus cable length.

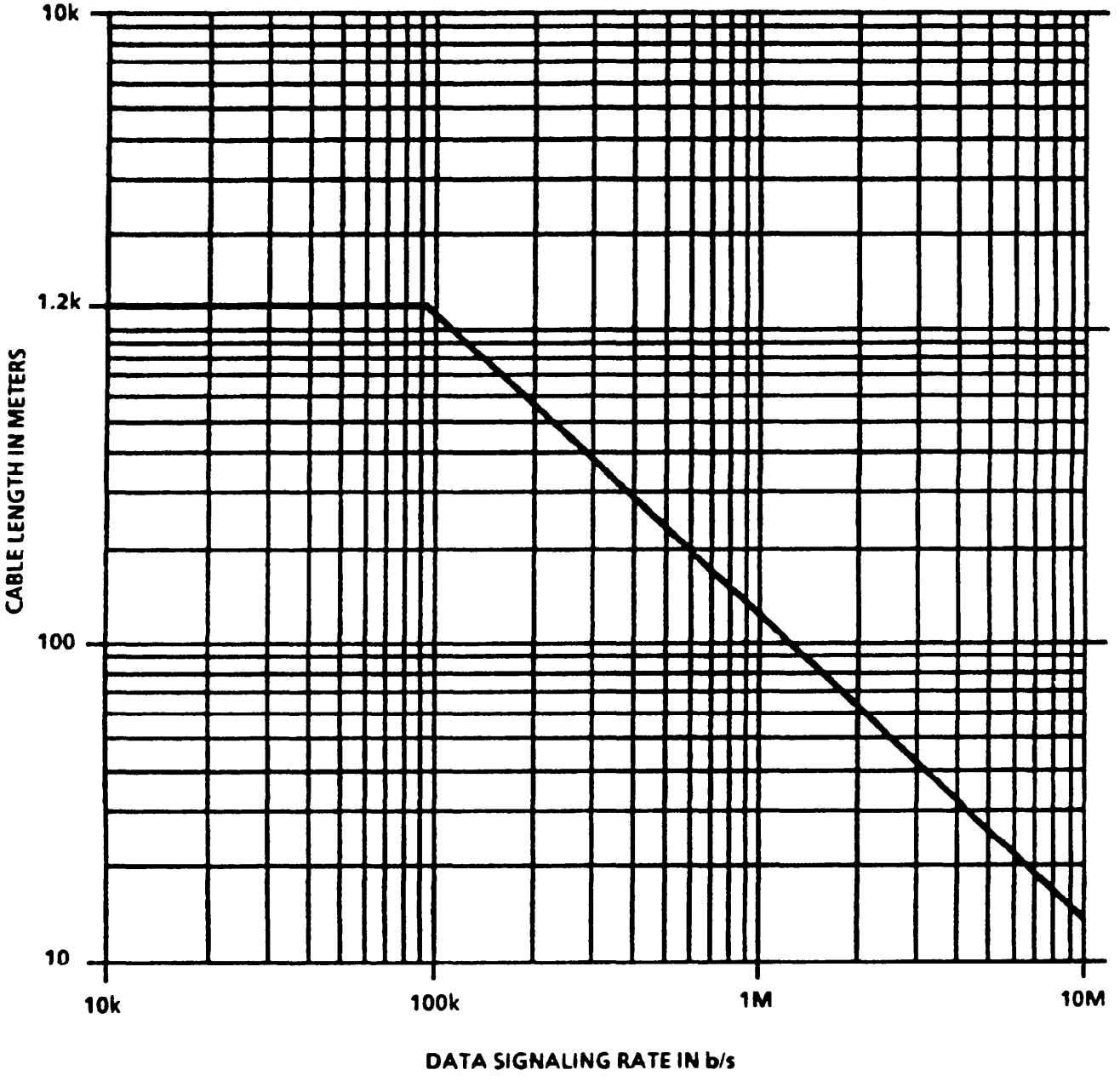


FIGURE 20. Signaling rate versus cable length for balanced voltage digital interface circuit.

than 0.05 unit interval, many applications can tolerate greater timing and amplitude distortion. Additionally, many applications can also tolerate a voltage loss of greater than 6 dB, as stated above. Thus, correspondingly greater cable lengths may be employed than those indicated. Experience has shown that in most practical cases the operating distance at lower signaling rates may be extended to several miles.

In selecting wire or cable for a given application, the resistance and capacitance per unit length should be considered. Figure 19 shows the cable RC time constant versus cable length for cable pairs with different characteristics. As long as the signal rise time allows the signal to achieve full amplitude within the unit interval, cable capacitance normally will not be a problem. Conservative design would limit the rise time to less than 30 percent of the unit interval.

30.4 Wire or cable termination resistance. For type I and type II generators (see 4.4.1), the use of a wire or cable termination is optional and dependent on the specific application. At the higher signaling rates (above 200 kb/s) or at any signaling rate where the propagation delay of the wire or cable is on the order of half the data unit interval, a termination should be used to preserve the signal rise time and to minimize reflections. The terminating impedance should match as closely as possible the characteristic impedance of the wire or cable in the signal spectrum transmitted. As a general rule, whenever there are multiple receivers connected to the line, the termination should be associated with the line and not with a specific receiver, otherwise removal or replacement of a receiver could also remove the termination or result in multiple terminations.

The characteristic impedance of twisted pair wire or cable is a function of frequency, wire size and type, as well as the kind of insulation materials employed. For example, the characteristic impedance of average 24 AWG copper conductor, plastic insulated twisted pair telephone cable, to a 100 kHz sine wave will be on the order of 100 ohms.

Generally, a resistance in the range of 120 ohms to 150 ohms will be satisfactory, the higher values leading to lower power dissipation. (See 5.2.3.6).

At lower signaling rates, where zero-voltage crossing ambiguity and signal rise time are not critical, the wire or cable need not be terminated. Therefore, no termination resistance is required or specified for the unbalanced voltage digital interface circuit.

30.5 Fail-safe operation. It may be required that specific interface leads be made fail-safe to certain fault conditions. The method of providing fail-safe is not standardized. An example of fail-safe operation for the unbalanced and the balanced voltage digital interface circuit is given in 30.5.1 and 30.5.2, respectively.

30.5.1 Example of fail-safe operation for unbalanced voltage digital interface circuit. The circuit shown in Figure 21 as an example, will provide a steady binary condition of a single receiver for the following fault conditions:

a. Generator power off.

b. Open signal lead (signal common return still connected).

c. Generator not implemented (signal lead may or may not be present).

d. Open connector (both signal lead and the signal common return are open simultaneously).

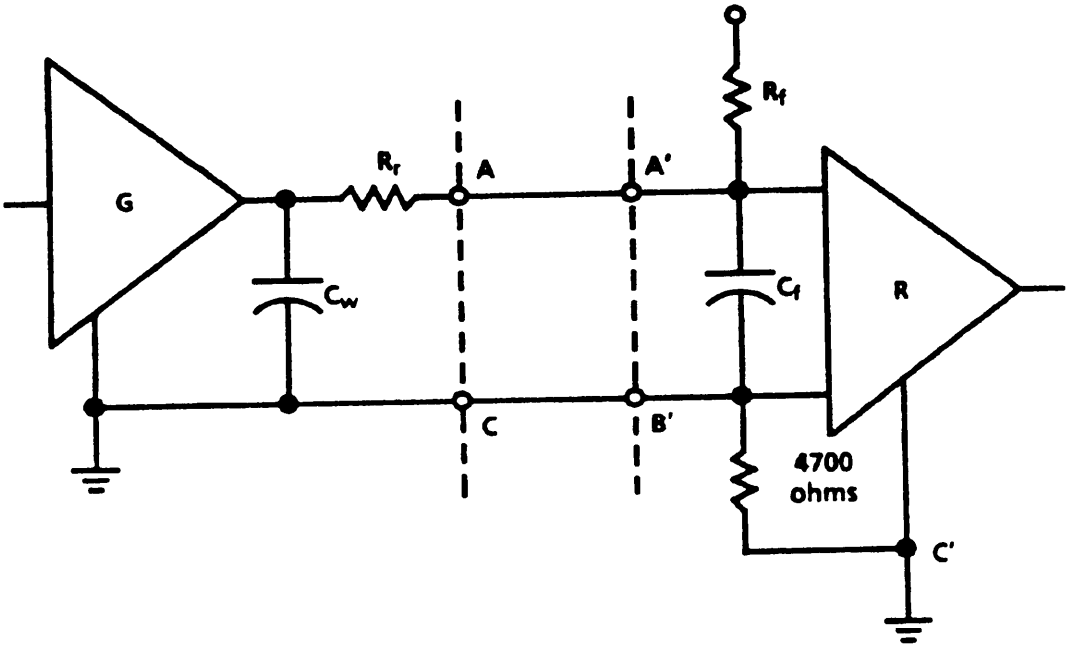
The fail-safe circuit in Figure 21 uses a bias voltage through a resistance to detect faults a through d above. Under low generator resistance conditions (normal operation), the bias voltage V_f has little effect on the receiver operation. Under high generator resistance conditions (fail), the bias forces the receiver to the desired binary steady-state condition. The capacitor C_f is required in the load to reduce any spurious noise, as a result of near-end crosstalk, to an ineffective level. The suggested values for C_f that will have little effect on normal operation are also given in Figure 21. If RC waveshaping as described in 5.1.1.8 is employed, an additional 50-ohm resistor R_r should be added in series with the generator output to reduce the effect of reflected waves.

If the fail-safe is implemented by other methods, additional fault conditions may be detected. For example, a threshold region detector (a window detector to respond when the input signal lies within the -200 mV to +200 mV transition region) in conjunction with a monostable timing device to determine when such a condition (input signal within the transition region) has existed for an abnormal amount of time, will expand fault coverage to include a shorted wire or cable pair (in addition to detecting faults a through d above). The user is cautioned that auxiliary circuits attached to perform the functions outlined above must not cause the shunt resistance of the load (A' to B' of Figure 21) to be less than 400 ohms. (See 5.1.3.6.) In addition, such auxiliary circuits must be capable of operating over the ranges of input voltages specified for a receiver in 5.1.3.1 through 5.1.3.3.

30.5.2 Example of fail-safe operation for balanced voltage digital interface circuit. The circuit shown in Figure 22 as an example, will provide a steady binary condition of a single receiver for the following fault conditions:

a. Generator power off.

b. Both signal wires open. (Signal common return still connected.)

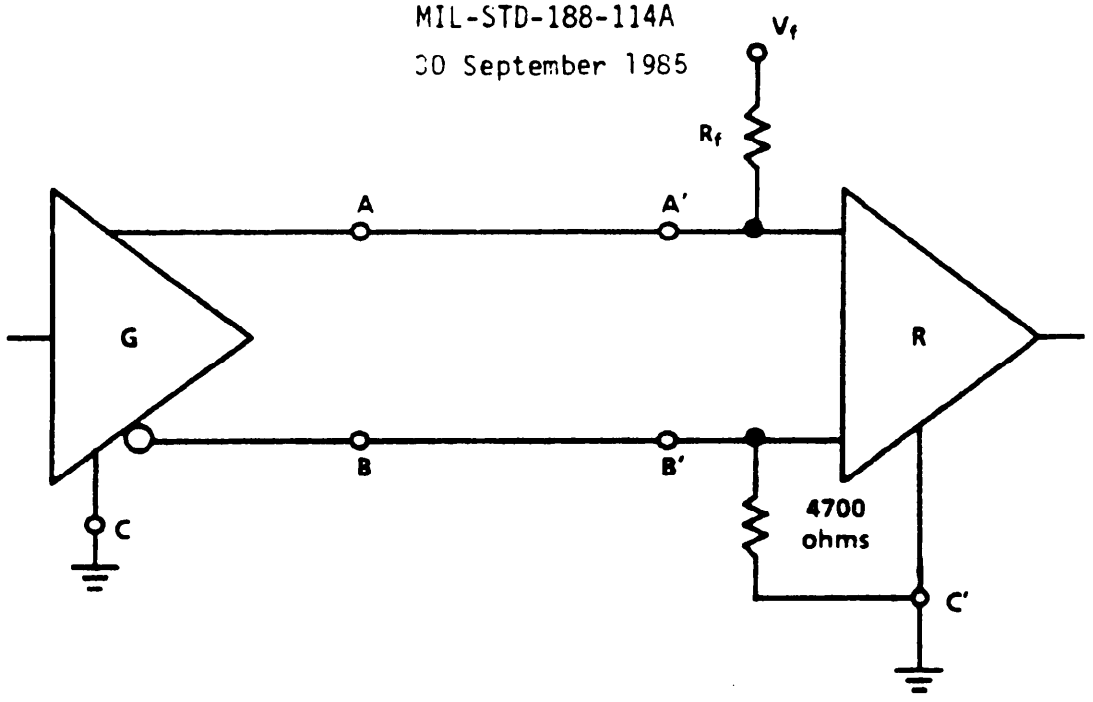


MAXIMUM SIGNALING RATE (kb/s)	C_f (MICROFARADS)
0 - 2.5	0.22
2.5 - 5	0.10
5 - 10	0.05
10 - 25	0.022
25 - 50	0.010
50 - 100	0.005

R_r = 50 ohms
FOR C_w SEE FIGURE 7

4 V ≤ $|V_f|$ ≤ 10 V
R_f = $|V_f|$ X 1000 ohms, ± 10 PERCENT

FIGURE 21. Example method of fail-safe for unbalanced voltage digital interface circuit.



LEGEND: $R_f = |V_f| \times 100$ ohms, ± 10 PERCENT

$4V \leq |V_f| \leq 10V$

FIGURE 22. Example method of fail-safe for balanced voltage digital interface circuit.

c. Generator not implemented (signal leads may or may not be present).

d. Open connector (both signal leads and the common signal return are open simultaneously).

The fail-safe circuit in Figure 22 uses two resistors and a voltage source as shown to produce a steady bias on the receiver in the event of any of the faults a through d listed above. In normal operation, the low source resistance of the generator will cause the effect of the bias to become negligible on the receiver slicing level. This circuit will not protect against short circuits across the wire or cable pair, nor will it protect against single open ground returns, and is not applicable where a termination resistance R_t is used.

If the fail-safe is implemented by other methods, additional fault conditions may be detected. For example, a threshold region detector (a window detector to respond when the input signal lies within the -200 mV to +200 mV transition region) in conjunction with a monostable timing device to determine when such a condition (input signal within the transition region) has existed for an abnormal amount of time, will expand fault coverage to

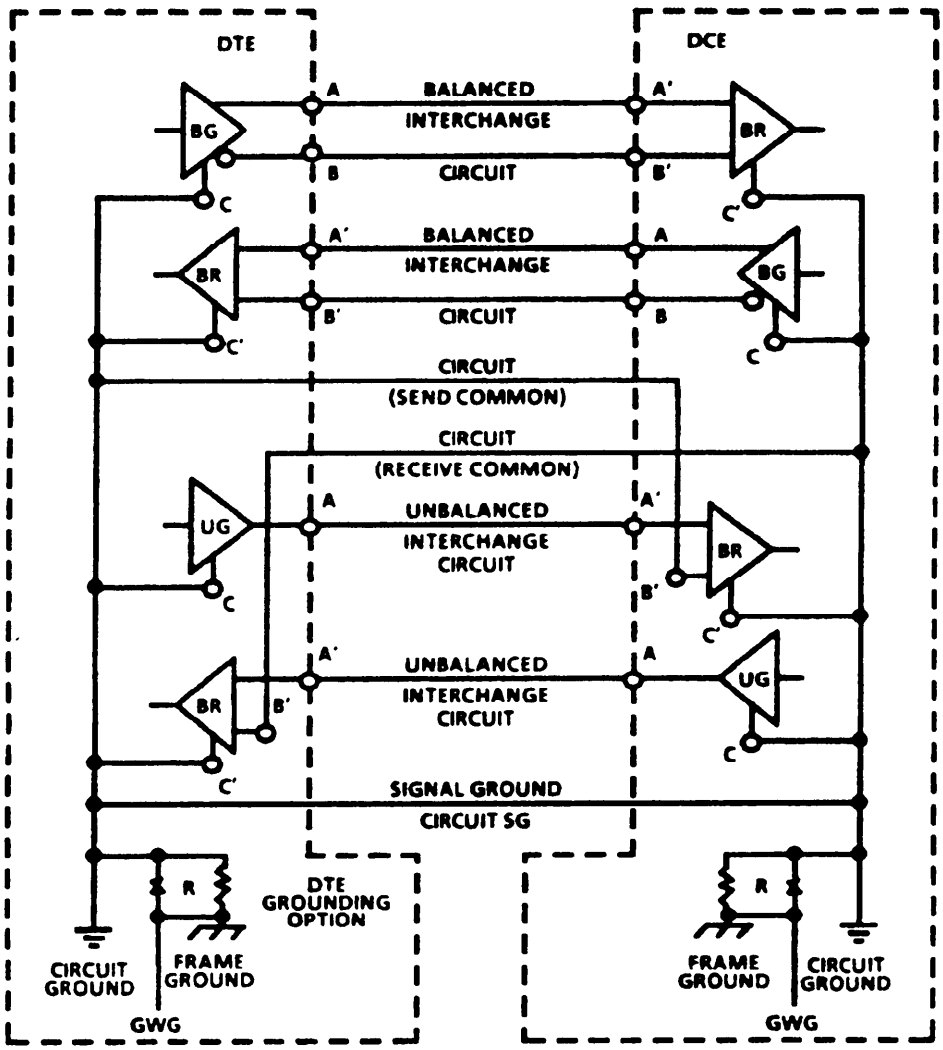
include a shorted wire or cable pair (in addition to detecting faults a through d above) and could be used when the wire or cable termination resistance is present. The user is cautioned that auxiliary circuits attached to perform the functions outlined above must not cause the shunt resistance of the load (A' to B' of Figure 22) to be less than 120 ohms (see 5.2.3.6). In addition, such auxiliary circuits must be capable of operating over the ranges of input voltages specified for a receiver in 5.1.3.1 through 5.1.3.3.

30.6 Optional grounding arrangements. In addition to the mandatory grounding requirements of MIL-STD-188-124 (see 4.6), this paragraph provides optional grounding arrangements applicable to digital interface circuits. Proper operation of the interface circuits, whether using balanced, unbalanced, or a combination of balanced and unbalanced electrical characteristics, requires the presence of a path between the circuit grounds of the equipment at each end of the interconnection. For example, in a DTE/DCE interface as shown in Figure 23, this path may be obtained in a number of ways:

a. Through earth ground. In this case, both end equipments have their circuit ground connected to frame ground which in turn is connected to earth ground (e.g., through the third wire or green wire ground (GWG) of the power cord). This is the preferred arrangement when the two earth grounds are at a potential difference of less than four volts.

b. By connecting circuit SC (send common) to DCE circuit ground by means of a wiring option in the DCE. To avoid circulating ground currents, circuit ground must be separated from frame ground in the DCE when this connection is made. Thus, circuit ground for the DCE is obtained from the DTE circuit ground through the interface circuit SC. The DCE must be capable of withstanding the resulting ground potential differences between its circuit ground and its frame ground. This is the preferred arrangement when the two earth grounds are at a potential difference greater than four volts and the DTE earth ground is the "quieter" of the two earth grounds.

c. By connecting circuit RC (receive common) to DTE circuit ground by means of a wiring option in the DTE. To avoid circulating ground currents, circuit ground must be separated from frame ground in the DTE when this connection is made. Thus, the circuit ground for the DTE is obtained from the DCE circuit ground through interface circuit RC. The DTE must be capable of withstanding the resulting ground potential differences between its circuit ground and its frame ground. This is the preferred arrangement when the two earth grounds are at a potential difference greater than four volts and the DCE earth ground is the "quieter" of the two earth grounds.



LEGEND:
- BG = BALANCED GENERATOR
- BR = BALANCED RECEIVER
- UG = UNBALANCED GENERATOR
- DTE = DATA TERMINAL EQUIPMENT
- DCE = DATA COMMUNICATIONS TERMINATING EQUIPMENT
- X = SWITCHED OR PATCHED CONNECTION (SEE 30.6)
- R = RESISTOR, 100 ohms, ± 20 PERCENT, ½ WATT (SEE 30.6.d)
- GWG = GREEN WIRE GROUND

FIGURE 23. Examples of optional grounding arrangements.

d. The connection between circuit ground and frame ground may be made through a 100-ohm, ±20 percent, one-half watt resistor. When used, a provision should be made to allow bypassing of the resistor for direct connection when needed for specific installations. Under ground fault conditions the resistor may fail and provisions should be made for inspection and replacement. Care should be used to prevent high ground loop currents.

30.6.1 Signal common return for unbalanced voltage digital interface circuit. (See Figure 24.) The interconnection between the generator and load interface points shown in Figure 24 consists of a signal conductor and a signal common return. In order to minimize the effects of ground potential difference (V_g) and longitudinally coupled noise on the signal at the load interface point, the signal return should only be connected to circuit ground at the terminal C of the generator interface point. (See 30.6 for optional signal and protective grounding arrangements). Two possible configurations for interconnection of signal return conductors for unbalanced voltage digital interface circuits are shown in Figure 24. In configuration 1, separate signal return conductors are used for each receiver. Configuration 1 has the advantage that it may be easily connected to balanced as well as unbalanced generators. Signal common returns may be shared, as shown in configuration 2 of Figure 24, however, a separate signal return should be used for each signal direction in an interconnection. For example, the terminal B' of all receivers in the DTE that interconnect with unbalanced generators in the DCE should connect to the receive common signal return which is only connected to generator circuit ground (terminal C) in the DCE. Similarly, the send common signal return is used to interconnect the terminal B' of all receivers in the DCE with the generator circuit ground (terminal C) in the DTE.

In older digital interface standards, a single signal ground conductor, which connected the circuit ground of the DTE to the circuit ground of the DCE, was also used as a common signal return for unbalanced generators in both signal directions. This document requires a signal ground conductor to connect the generator circuit ground (terminal C) of the DTE to the generator circuit ground (terminal C) of the DCE, however, this conductor is not used as a signal return for unbalanced circuits. (See 5.4 and 40.)

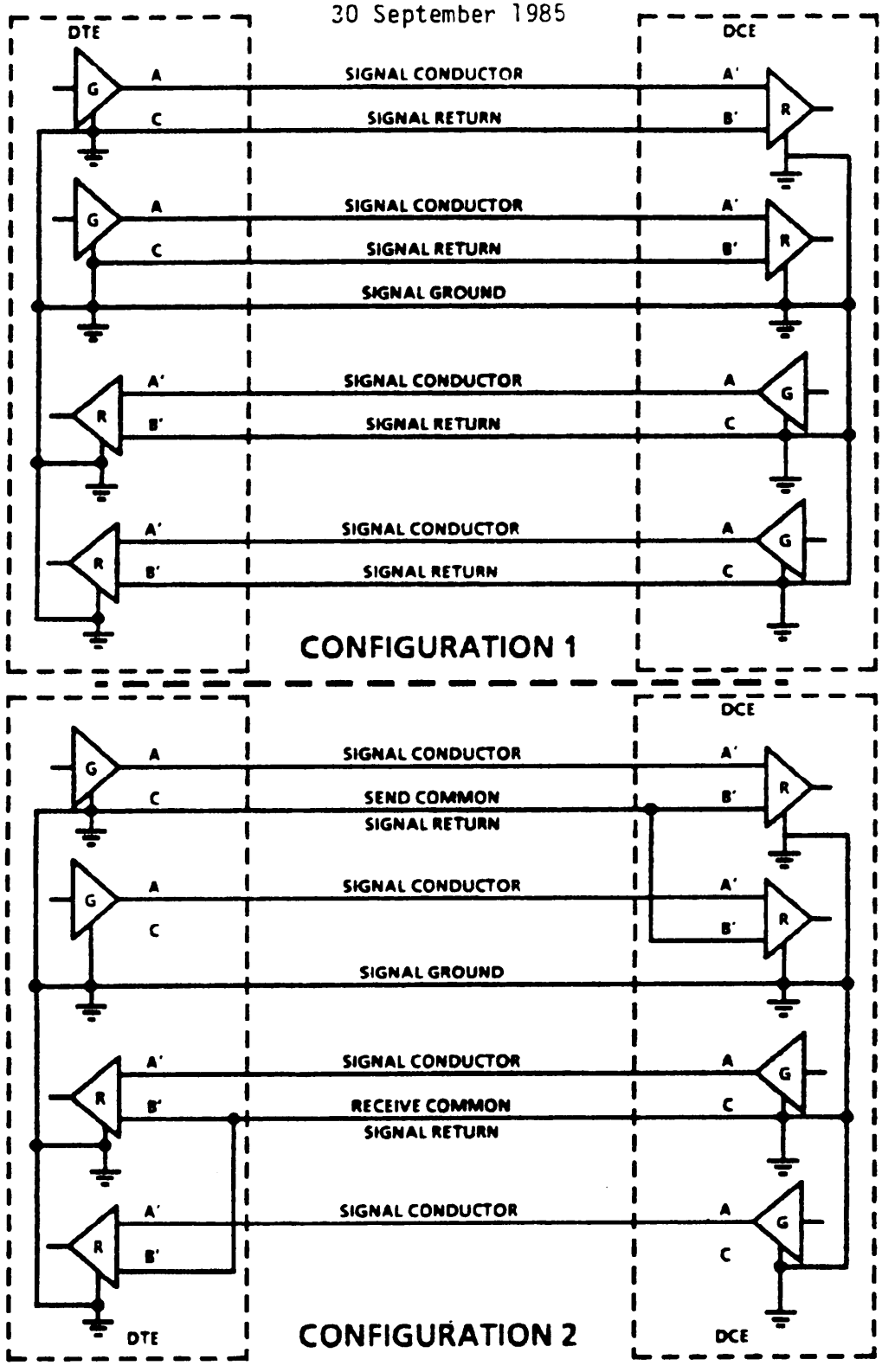


FIGURE 24. Interconnection of signal common return for unbalanced voltage digital interface circuit.

APPENDIX D
GUIDELINES ON INTEROPERATION AMONG DEVICES COMPLYING WITH DIFFERENT LOW LEVEL DIGITAL INTERFACE STANDARDS

40. GENERAL

40.1 Scope. This appendix contains guidelines on interoperation among devices complying with different low level digital interface standards. This appendix is not a mandatory part of MIL-STD-188-114A. The information contained herein is intended for guidance only.

40.2 Application. When interconnecting equipment using electrical characteristics specified in this document with interfaces using other electrical characteristics, consideration should be given to problems that may be encountered due to the different electrical charateristics.

40.3 Unbalanced voltage digital interface standards. Basically, the older EIA Standard RS-232C has been modified by RS-423 and RS-423A to essentially the same electrical characteristics as the MIL-STD-188C and the MIL-STD-188-100 Unbalanced Low Level Digital Interfaces which have been superseded by MIL-STD-188-114. The EIA RS-232C interface circuit recommends that the length of the interconnecting wire or cable be limited to 50 feet. This limitation has been removed by the EIA Standard RS-423A. The EIA Standard RS-423A has been adopted as FED-STD-1030A which is compatible with MIL-STD-188-114A (see also 4.4). The RS-232C generator may have outputs as high as plus or minus 25 volts, therefore, voltage attenuators may be required to permit interoperation with FED-STD-1030A or MIL-STD-188-114A receivers.

The significant difference between the MIL-STD-188C or MIL-STD-188-100 and the MIL-STD-188-114A unbalanced low level digital interface circuits is that the receiver in MIL-STD-188-114A has a balanced input, even though it is used with an unbalanced generator. The choice of a balanced receiver was done deliberately for the following specific reasons:

a. Noise immunity and reducing the problem of ground potential differences between generator and receiver(s).

b. Convenience of inverting the MARK and SPACE signal sense (see Note of 5.1.1.1).

c. Uniformity of receivers for economic advantages in mass production.

40.4 Balanced voltage digital interface standards. Basically, the balanced low level digital interface circuit contained in MIL-STD-188-100 and FED-STD-1020A (which adopts EIA Standard RS-422A) is the same as the balanced voltage digital interface circuit contained in MIL-STD-188-114A. The significant electrical difference between MIL-STD-188-114A and FED-STD-1020A is the permitted generator offset voltage for type I generators (see 4.4.1). The permitted 3-volt generator offset of FED-STD-1020A is limited to 0.4

volts in MIL-STD-188-114A for type I generators operating below 100 kb/s. The reason for this limitation is the necessary interoperability and compatibility among existing older interface circuits designed in accordance with MIL-STD-188C and MIL-STD-188-100 and newer circuits designed in accordance with MIL-STD-188-114 and MIL-STD-188-114A.

If the type I generator offset voltage would not be limited to 0.4 volts, an "engineered" incompatibility would exist between all older unbalanced receivers built in accordance with MIL-STD-188C or MIL-STD-188-100, and new balanced generators complying with MIL-STD-188-114A. In recognition that such an "engineered" incompatibility would have a severe technical and economical impact, MIL-STD-188-114A limits the permitted generator offset voltage for balanced interfaces operating at signaling rates below 100 kb/s. A level of 0.4 volts is considered a reasonable limit for mass production of integrated circuits and also an acceptable limit from the viewpoint of performance degradation of existing older unbalanced receivers.

40.5 Interfacing balanced or unbalanced generators with balanced or unbalanced receivers. Figures 25 through 30 are intended to convey the simplicity of interfacing generators and receivers, both balanced or unbalanced, that have been designed in accordance with MIL-STD-188, MIL-STD-188-100, MIL-STD-188-114, FED-STD-1020 or FED-STD-1030, or revisions.

A realistic way to approach the application engineering problem is:

a. To consider the generator (except the type III generator; see 4.4.1) as a low impedance source with an essentially constant voltage output,

b. To consider a typical field wire or telephone cable, at signaling rates below 20 kb/s and shorter than about 10,000 feet, as having an impedance dominated by the generator impedance, and

c. To consider the receiver as a voltage operated device that is isolated from the interconnecting wire or cable by a relatively high input resistance.

As the signaling rate or the operating distance, or both, are increased, more care and attention need to be given to the wire or cable termination problem. (See also 30.4.) It should be noted that at higher signaling rates the characteristic impedance of typical twisted pair telephone cable levels off to approximately 100 ohms.

While any balanced or unbalanced generator designed in accordance with MIL-STD-188C or MIL-STD-188-100 will operate correctly with a receiver designed in accordance with FED-STD-1020A, only those balanced generators of FED-STD-1020A with their offset voltage limited to 0.4 volts will operate correctly with any MIL-STD-188C or MIL-STD-188-100 unbalanced receiver. New MIL-STD-188-114A receivers will operate correctly with MIL-STD-188C or MIL-STD-188-100 generators. These relationships regarding interoperability are shown in matrix form in Table IV.

40.5.1 Examples of interfacing unbalanced generators with balanced or unbalanced receivers. Figure 25 shows how an unbalanced generator designed in accordance with MIL-STD-188C, MIL-STD-188-100 or MIL-STD-188-114A is connected to an unbalanced receiver designed in accordance with MIL-STD-188C or MIL-STD-188-100. Figure 26 depicts the same generator as shown in Figure 25 connected to a balanced receiver, designed in accordance with MIL-STD-188-100 or MIL-STD-188-114A, without inversion of the MARK-SPACE signal sense; whereas Figure 27 shows the same configuration as Figure 26 except the MARK-SPACE signal sense is inverted by changing the connections at the balanced receiver input.

Figure 28 shows a method for obtaining essentially all the operating advantages of balanced operation when only an unbalanced generator is available. This circuit has the additional advantage that the unbalanced generator can be replaced by a balanced generator at a later date, without changing the interconnecting wire or cable, the patch and test facilities, and other related hardware.

40.5.2 Examples of interfacing balanced generators with balanced or unbalanced receivers. Figure 29 depicts a typical balanced interface circuit with wire or cable termination resistance R_t. The purpose of the termination resistance is to minimize reflections in the wire or cable at higher signaling rates (see 5.2.3.7 and 5.3.3.7).

As shown in Figure 30, the interfacing of a balanced generator to an older unbalanced receiver designed in accordance with MIL-STD-188C or MIL-STD-188-100 requires that the offset voltage of the balanced generator be limited to a value that insures a signal voltage zero crossing of the generator with respect to the zero voltage reference of the receiver input. The magnitude of the zero crossing signal should be sufficient to overcome any noise or signal waveshape ambiguity. In recognition of the need for sufficient operating margin, a maximum generator offset voltage of 0.4 volts was chosen for the type I generator (see 4.4.1). The use of a balanced generator with an unbalanced receiver results in half the signal amplitude available from the balanced generator. Therefore, equipment expected to interface with unbalanced receivers should have provision for an unbalanced generator, if possible, to permit a higher input signal at the receiver.

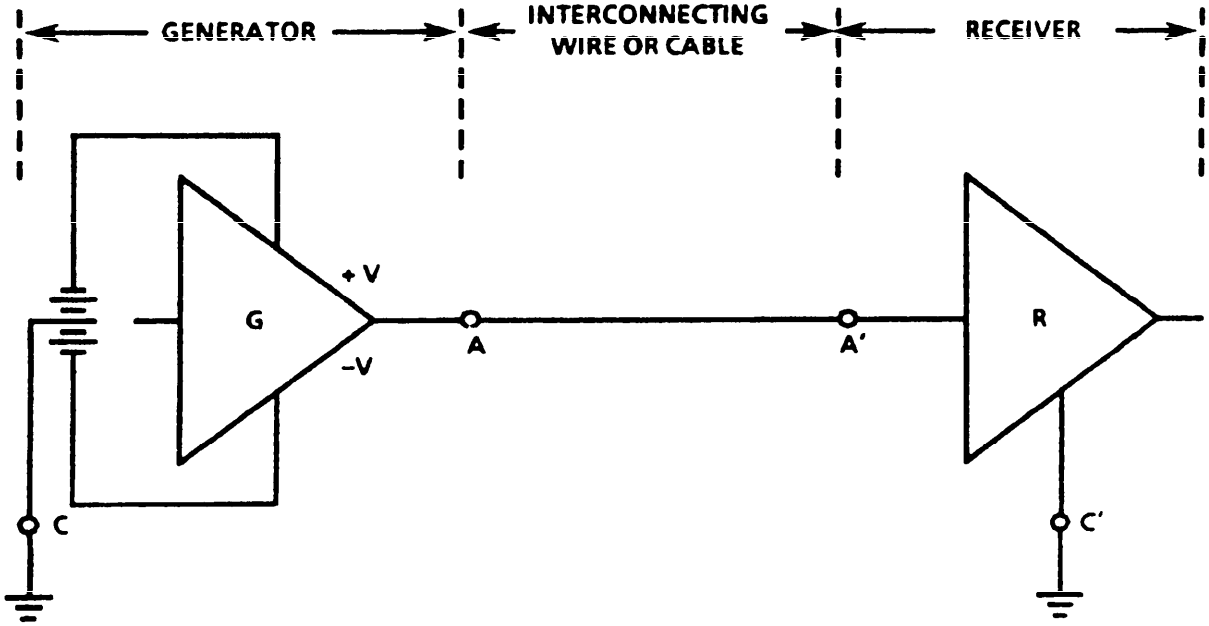


FIGURE 25. Unbalanced generator driving unbalanced receiver.

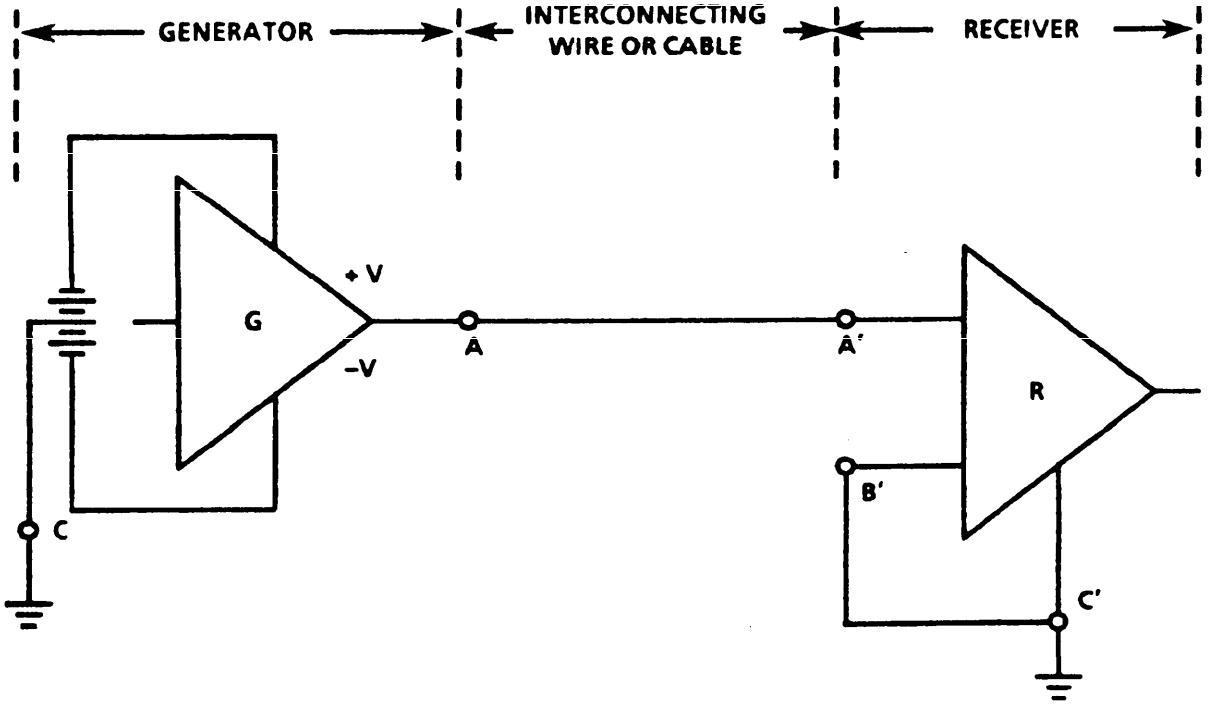


FIGURE 26. Unbalanced generator driving balanced receiver without inversion of MARK-SPACE signal sense.

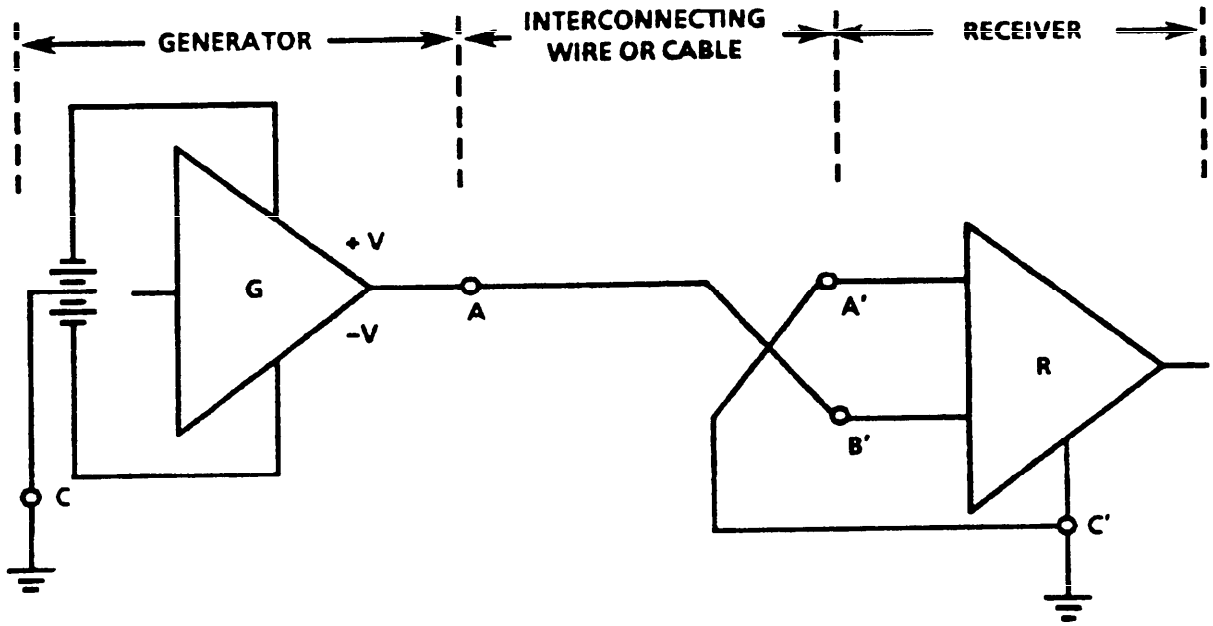
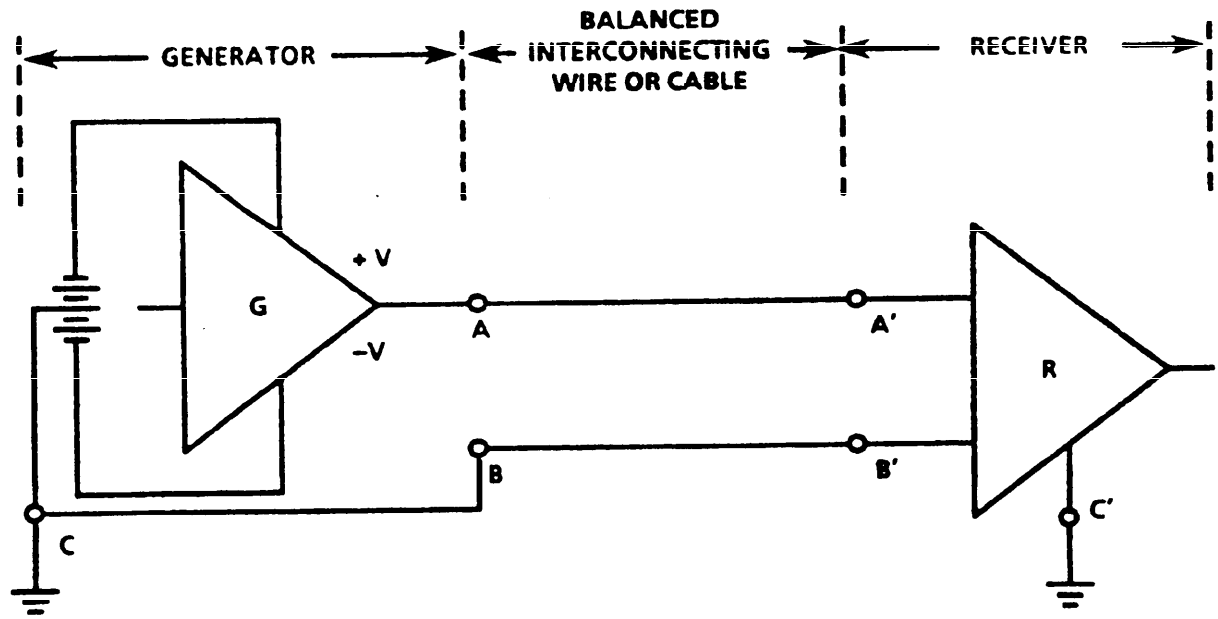


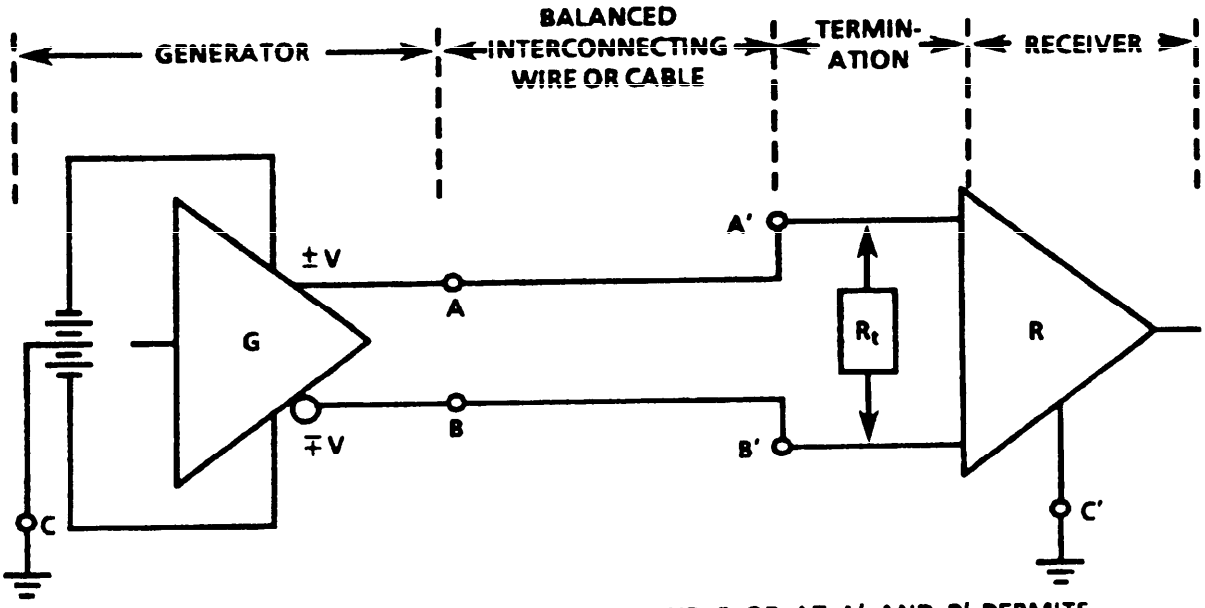
FIGURE 27. Unbalanced generator driving balanced receiver with inversion of MARK-SPACE signal sense.



NOTE 1: REVERSING WIRE CONNECTIONS AT A AND B OR AT A' AND B' PERMITS INVERSION OF MARK-SPACE SIGNAL SENSE.

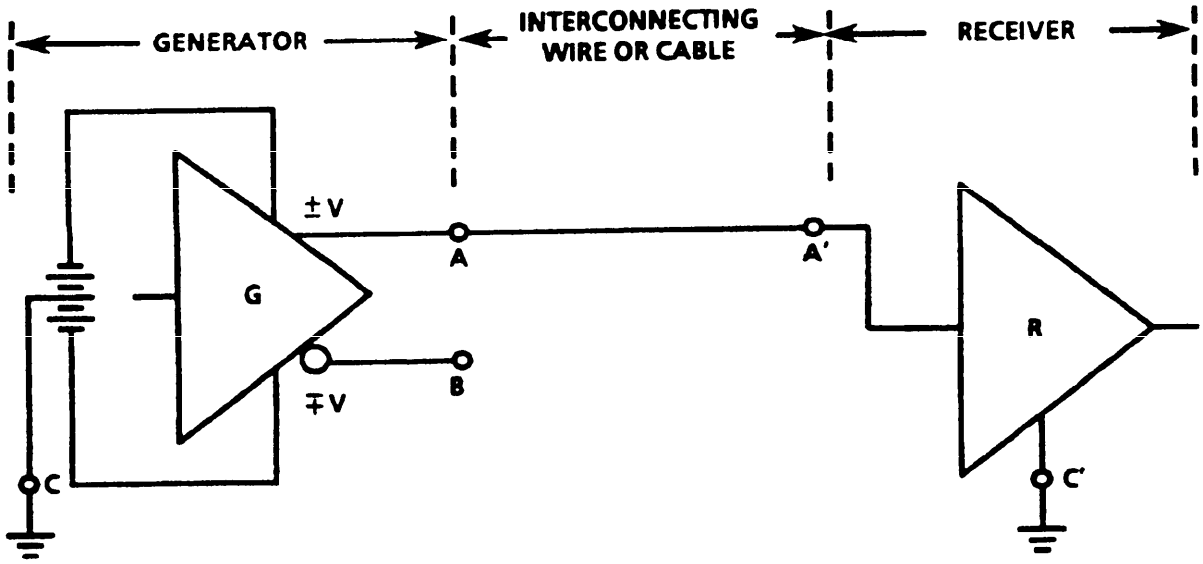
NOTE 2: THIS MODE OF OPERATION HAS ESSENTIALLY ALL OF THE ADVANTAGES OF BALANCED OPERATION REGARDING NOISE IMMUNITY AND GROUND POTENTIAL DIFFERENCES.

FIGURE 28. Unbalanced generator driving balanced wire pair with balanced receiver.



NOTE 1: REVERSING WIRE CONNECTIONS AT A AND B OR AT A' AND B' PERMITS INVERSION OF MARK-SPACE SIGNAL SENSE.
NOTE 2: SEE 30.2 ON NEED FOR PROVIDING WIRE OR CABLE TERMINATION RESISTANCE.

FIGURE 29. Balanced generator driving balanced receiver.



NOTE 1: THIS MODE OF OPERATION REQUIRES THE BALANCED GENERATOR OFFSET VOLTAGE TO BE LIMITED TO 0.4 VOLTS. (TYPE I GENERERATOR).
NOTE 2: CONNECTING THE RECEIVER TO TERMINAL B PERMITS INVERSION OF MARK-SPACE SIGNAL SENSE.

FIGURE 30. Balanced generator driving unbalanced receiver.

TABLE IV. Interoperation among devices complying with different low level digital interface standards.

		MIL-STD 188C		MIL-STD-188-100				MIL-STD-188-114A				FED-STD-1020A		FED-STD-1030A	
		UG	UR	BG	UG	BR	UR	BGI	BGII	UG	BR	BG	BR	UG	BR
MIL-STD-188C	UG	0	X	0	0	X	X	0	0	0	X	0	X	0	X
	UR	X	0	X	X	0	0	X	I	X	0	I	0	X	0
MIL-STD-188-100	BG	0	X	0	0	X	X	0	0	0	X	0	X	0	X
	UG	0	X	0	0	X	X	0	0	0	X	0	X	0	X
	BR	X	0	X	X	0	0	X	X	X	0	X	0	X	0
	UR	X	0	X	X	0	0	X	I	X	0	I	0	X	0
MIL-STD-188-114A	BGI	0	X	0	0	X	X	0	0	0	X	0	X	0	X
	BGII	0	I	0	0	X	I	0	0	0	X	0	X	0	X
	UG	0	X	0	0	X	X	0	0	0	X	0	X	0	X
	BR	X	0	X	X	0	0	X	X	X	0	X	0	X	0
FED-STD-1020A	BG	0	I	0	0	X	I	0	0	0	X	0	X	0	X
	BR	X	0	X	X	0	0	X	X	X	0	X	0	X	0
FED-STD-1030A	UG	0	X	0	0	X	X	0	0	0	X	0	X	0	X
	BR	X	0	X	X	0	0	X	X	X	0	X	0	X	0

LEGEND:
- I = Interoperation possible if balanced generator offset voltage is limited to 0.4 volts (see 5.2.1.4) and correct signal sense is observed (see 5.1.1.1).
- X = Direct interoperability (see 4.5) except for possible inversion of signal sense (see 5.1.1.1).
- 0 = Not applicable.
- BG = Balanced Generator
- UG = Unbalanced Generator
- BR = Balanced Receiver
- UR = Unbalanced Receiver
- BGI = Type I Balanced Generator (see 4.4.1)
- BGII = Type II Balanced Generator (see 4.4.1)

NOTE 1: Type III balanced generators may be considered equivalent to type I balanced generators in order to determine interoperability, however signaling rate and termination differences must be considered. (See 5.3.)

NOTE 2: FED-STD-1030A may be considered equivalent to EIA RS-423A and CCITT Recommendation V.10.

NOTE 3: FED-STD-1020A may be considered equivalent to EIA RS-422A and CCITT Recommendation V.11.

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