INCH-POUND
MIL-PRF-32535
28 September 2015

PERFORMANCE SPECIFICATION

CAPACITOR, CHIP, FIXED, CERAMIC DIELECTRIC (TEMPERATURE STABLE AND GENERAL PURPOSE), EXTENDED RANGE, HIGH RELIABILITY AND STANDARD RELIABILITY, GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for extended range, general purpose and temperature stable, surface mount, ceramic capacitors. Two product levels are offered: M level (standard reliability) and T level (high reliability). T level capacitors are intended for space, missile, and other high reliability applications. MIL-PRF-32535 capacitors have higher capacitance values than MIL-PRF-123 and MIL-PRF-55681 capacitors of the same size and voltage rating.

1.2 Classification.

1.2.1 Part or Identifying Number (PIN). Capacitors specified herein (see 3.1) are identified by a PIN which consists of a product level identifier followed by the basic number of the performance specification sheet and a series of coded characters. Each performance specification sheet covers a different capacitor size. The coded number provides information concerning the capacitors' characteristic, working voltage, capacitance value, capacitance tolerance, termination, and electrode material. The PIN is in the following form:

M32535	01	BX	B	103	K	Z	M	B 1/
Performance specification number	Slash sheet number	Characteristic (see 1.2.1.1)	Voltage (see 1.2.1.2)	Capacitance (see 1.2.1.3)	Capacitance tolerance (see 1.2.1.4)	Termination (see 1.2.1.5)	Product level (see 1.2.1.6)	Electrode (see 1.2.1.7)

1/ When a specific electrode material is not required, the electrode designator is left blank (see 1.2.1.7).

1.2.1.1 Characteristic. The characteristic refers to the voltage-temperature limits (VTL) or temperature characteristic (TC) of the capacitor, as applicable. For two character characteristics, the first letter (B) identifies the rated temperature range of -55°C to +125°C. The second letter indicates the voltage-temperature limits as shown in table I. The class and three character characteristics (C0G, X7R, and X7S) are defined in ECIA EIA-198-1.

1.2.1.2 Voltage. The rated voltage for continuous operation at +125°C is identified by a single letter as shown in table II.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAT, Post Office Box 3990, Columbus, OH 43218-3990, or emailed to capacitorfilter@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

TABLE I. Voltage-temperature limits / temperature characteristic.

Symbol	Characteristic	Class	Capacitance change with reference to +25°C		
			Steps A through D of table XXIII	Percent rated voltage	Steps E through G of table XXIII
BG	BG	I	90 ±20 ppm/°C	100	90 ±20 ppm/°C
BP	BP	I	0 ±30 ppm/°C	100	0 ±30 ppm/°C
E1	C0G	I	0 ±30 ppm/°C	N/A	N/A
BR	BR	II	±15 percent	100	+15, -40 percent
BX	BX	II	±15 percent	100	+15, -25 percent
BZ	BZ	II	±15 percent	60	+15, -45 percent
BN	BN	II	±15 percent	50	+15, -60 percent
E2	X7R	II	±15 percent	N/A	N/A
E3	X7S	II	±22 percent	N/A	N/A

TABLE II. Rated voltage.

Symbol	Rated voltage (V_{dc})
V	4
W	6.3
X	10
Y	16
Z	25
A	50
B	100
C	200

1.2.1.3 Capacitance. The nominal capacitance value, expressed in picofarads (pF) is identified by a three digit number; the first two digits represent significant figures and the last digit specifies the number of zeros to follow. When the nominal value is less than 10 pF, the letter “R” is used to indicate the decimal point and the succeeding digit(s) of the group represent significant figure(s). 1R0 indicates 1.0 pF; R75 indicates .75 pF; and 0R5 indicates 0.5 pF.

1.2.1.4 Capacitance tolerance. The capacitance tolerance is identified by a single letter as shown in table III.

TABLE III. Capacitance tolerance.

Symbol	Capacitance tolerance (±)
B	0.1 pF
C	0.25 pF
D	0.5 pF
F	1 percent
G	2 percent
J	5 percent
K	10 percent
M	20 percent

1.2.1.5 Termination. The termination material is identified by a single letter as shown in table IV.

TABLE IV. Termination.

Symbol	Termination type
D	Base metallization – nickel – solder dipped (tin/lead alloy with a minimum of 3 percent lead).
G	Base metallization - nickel – gold plated
M 1/	Palladium/silver alloy (only available with precious metal electrodes)
R	Base metallization – conductive epoxy – nickel – solder plated (tin/lead alloy with a minimum of 3 percent lead)
V	Base metallization – conductive epoxy - nickel - gold plated
Z	Base metallization – nickel - solder plated (tin/lead alloy with a minimum of 3 percent lead)

1/ Termination M is intended to be mounted with a conductive adhesive.

1.2.1.6 Product level. The product level is identified by a single letter as shown in table V.

TABLE V. Product level.

Symbol	Product level
M	Standard reliability
T	High reliability

1.2.1.7 Electrode. The electrode material is identified by a single letter or left blank as shown in table VI.

TABLE VI. Electrode material.

Symbol	Electrode material
P	Precious metal electrode (PME), palladium/silver
B	Base metal electrode (BME), nickel
Blank 1/	PME or BME

1/ For ordering purposes only. Package marking will include the electrode material symbol (see 3.22.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

(See supplement 1 for list of associated specification sheets.)

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202	-	Electronic and Electrical Component Parts, Test Methods for
MIL-STD-790	-	Standard Practice for Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications
MIL-STD-883	-	Microcircuits, Test Methods for

(Copies of these documents are available online at http://quicksearch.dla.mil/.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONIC COMPONENTS INDUSTRY ASSOCIATION (ECIA)

ECIA EIA/ECA-469	-	Standard Test Method for Destructive Physical Analysis (DPA) of Ceramic Monolithic Capacitors

(Copies of these documents are available from http://www.ecianow.org.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related associated specifications, specification sheets, or MS sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of any conflict between requirements of this specification and the specification sheet, the latter shall govern.

3.2 Qualification. Capacitors furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified products list at the time of award of contract (see 4.4 and 6.3).

3.3 Qualified Product List (QPL) system. The manufacturer shall establish and maintain a QPL system for capacitors covered by this specification. This QPL system shall be established and maintained in accordance with the procedures and requirements specified in MIL-STD-790 and herein.

3.4 Interface and physical dimensions. Capacitors shall meet the interface and physical dimensions specified (see 3.1).

3.4.1 Pure tin. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. Tin content of capacitor components and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see 6.7).

3.5 Ultrasonic inspection. When examined in accordance with 4.6.1, all responses shall be rejected, except in the case of false responses (see C.1.2.4). If false responses are suspected, the manufacturer may individually examine the capacitor and accept it if the false response is confirmed.

3.6 Visual examination. When examined in accordance with 4.6.2, capacitors shall meet the visual requirements specified in appendix B.

3.7 Thermal shock and voltage conditioning. When tested in accordance with 4.6.3, capacitors shall withstand the extremes of high and low temperature without visible damage and meet the following requirements with the percent defective allowed as shown in table XVII:

a. Insulation resistance (at +125°C): Shall be not less than the initial requirement (see 3.8).

b. Dielectric withstanding voltage (at +25°C): In accordance with 3.9.

c. Insulation resistance (at +25°C): Shall be not less than the initial requirement.

d. Capacitance (at +25°C): Shall be within the tolerance specified (see 3.1).

e. Dissipation factor (at +25°C): Shall not exceed the value specified (see table VII).

NOTE: Capacitance and dissipation factor failures shall be removed from the lot but shall not be considered defective for the determination of the percent defective allowed (see 4.5.2.2.1.1 and table XVII).

3.8 Insulation resistance (IR). Unless otherwise specified (see 3.1), when measured in accordance with 4.6.4, the insulation resistance shall be not less than the value specified:

a. For capacitors rated 25 V_{dc} and higher:

(1) At +25°C: 100,000 megohms or 1,000 megohm-microfarads, whichever is less.

(2) At +125°C: 10,000 megohms or 50 megohm-microfarads, whichever is less.

b. For capacitors rated less than 25 V_{dc}:

(1) At +25°C: 100,000 megohms or 500 megohm-microfarads, whichever is less.

(2) At +125°C: 10,000 megohms or 50 megohm-microfarads, whichever is less.

3.9 Dielectric withstanding voltage (DWV). When tested in accordance with 4.6.5, there shall be no evidence of damage or breakdown.

3.10 Capacitance. When measured in accordance with 4.6.6, the capacitance shall be within the specified tolerance (see 3.1).

3.11 Dissipation factor (DF). When determined in accordance with 4.6.7, the dissipation factor shall not exceed the value specified in table VII.

TABLE VII. Dissipation factor limits.

Characteristic	Maximum allowable DF (%)					
	Rated Voltage (V_{dc})					
	4	6.3	10	16	25	≥50
Class II	7.5	7.5	5.0	3.5	3.5	2.5
BP, C0G (≥ 10 pf)	0.15	0.15	0.15	0.15	0.15	0.15
BP, C0G (< 10 pf)	0.25	0.25	0.25	0.25	0.25	0.25
BG (≥ 10 pf)	0.05	0.05	0.05	0.05	0.05	0.05
BG (< 10 pf)	0.15	0.15	0.15	0.15	0.15	0.15

3.12 Destructive physical analysis. When examined in accordance with 4.6.8, capacitors shall meet the requirements of ECIA EIA/ECA-469 with the following exceptions:

a. Defect criteria for delaminations (see 6.4.2):

(1) Any single fired-on delamination of an interface of material layers which exceeds 20% of the interface (pertaining to the overall chip element length or width), and exceeds .005 inch (0.127 mm) for case sizes larger than 0603 and exceeds .002 inch (0.051 mm) for case sizes 0603 and smaller.

(2) Any single delamination of an interface of material layers, in the active area, which exceeds .005 inch (0.127 mm) for case sizes larger than 0603 and exceeds .002 inch (0.051 mm) for a case sizes of 0603 and smaller, and displaces adjacent dielectric layers by more than 50% of the average dielectric thickness for the affected layer(s).

b. Defect criteria for margin defects:

(1) Side margins: Any side margin that displays a minimum margin less than the required minimum shown in table VIII.

TABLE VIII. Side margins.

Rated voltage (V_{dc})	Minimum side margin (in (mm))
4 through 6.3	.0006 (0.015)
10 through 16	.0008 (0.020)
25	.0010 (0.025)
> 25 through 50	.0016 (0.040)
> 50 through 200	.0020 (0.050)

(2) End margins: Any end margin with a minimum less than the values given in table IX.

TABLE IX. End margins.

Rated voltage (V_{dc})	Minimum end margin (in (mm))
4 through 6.3	.0010 (0.025)
10 through 16	.0014 (0.036)
25	.0016 (0.040)
> 25 through 50	.0020 (0.050)
> 50 through 200	.0030 (0.075)

(3) Cover plate thickness: Any cover plate with a minimum thickness less than the values given in table X.

TABLE X. Cover plate thickness.

Rated voltage (V_{dc})	Minimum cover plate thickness (in (mm))
4 through 6.3	.0010 (0.025)
10 through 16	.0014 (0.036)
25	.0016 (0.040)
> 25 through 50	.0020 (0.050)
> 50 through 200	.0030 (0.075)

c. Defect criteria for cracks (see 6.4.1) in the ceramic: Any crack in the dielectric of the active area or any crack in the enveloping ceramic margins/borders that either reduces, or has the potential, through further propagation, to reduce the effective margins to a point less than the limits defined by 3.12b.

d. Defect criteria for dielectric and electrode nonuniformities:

(1) Dielectric thickness is the actual measured thickness of the fired ceramic dielectric layer. Voids, or the cumulative effect of voids, shall not reduce the total dielectric thickness (T) by more than 30 percent (see figure 1). Inspection for 30% reduction in the thickness of an individual dielectric layer (see figure 1) shall not apply to dielectrics less than or equal to 7 microns.

NOTE: Inspection for 30% reduction in dielectric thickness for dielectrics less than or equal to 7 microns is not required due to lack of consistent and repeatable measurement.

FIGURE 1. Dielectric parameters.

(2) Undulations in the electrode and dielectric layers shall not be cause for rejection as long as both electrodes and dielectrics follow the same undulating pattern (see figure 2) without distorting the dielectric and the requirement of 3.12b is met.

FIGURE 2. Undulating electrode and dielectric layers.

3.13 Board flex. When tested in accordance with 4.6.9, capacitors shall meet the following:

a. Capacitance:

(1) During examination: Shall change not more than +/- 5% for class I dielectrics or +/- 10% for class II dielectrics.

(2) After examination: Shall be within the tolerance specified (see 3.1).

b. Dissipation factor: Shall not exceed the initial limit (see table VII).

c. Visual examination: There shall be no mechanical damage to the capacitor body, terminals, and body/terminal junction.

3.14 Shear stress. When capacitors are tested in accordance with 4.6.10, there shall be no evidence of cracking or of the capacitor being sheared from its pad.

3.15 Solderability. When capacitors are tested in accordance with 4.6.11, the immersed metallized surface shall be at least 85 percent covered with a smooth solder coating. The remaining 15 percent of the surface may contain small pinholes or exposed termination material; however, these shall not be concentrated in one area.

3.16 Bond strength (wire). When tested in accordance with 4.6.12, bond strength shall be at least 3.0 grams force, and there shall be no fracturing of the bond at the wire to electrode interface or separation of the electrode from the dielectric.

3.17 Resistance to soldering heat. When tested in accordance with 4.6.13, capacitors shall meet the following requirements:

a. Visual examination: There shall be no evidence of mechanical damage, or delamination, or exposed electrodes. Leaching shall be a maximum of 25 percent on each edge of mounting area (see figure 3).

b. Insulation resistance at +25°C: Not less than the initial +25°C requirement (see 3.8).

c. Capacitance:

(1) Class II characteristics: Shall change not more than -1.0 percent to +6.0 percent from the initial measured value.

(2) Class I characteristics: Shall change not more than -1.0 percent to +2.0 percent or 0.5 pF, whichever is greater, from the initial measured value.

d. Dissipation factor: Shall not exceed the initial limits (see table VII).

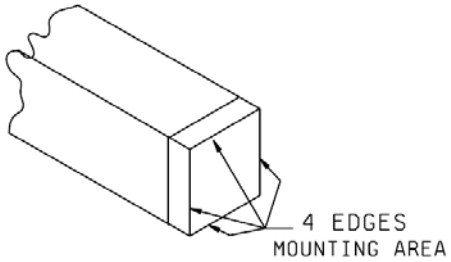


FIGURE 3. Mounting area.

3.18 Voltage-temperature limits / temperature characteristic. The capacitance change over the range of temperatures specified in 4.6.14 shall not exceed the limits specified in table I. The capacitance value obtained in step C of table XXIII shall be considered as the reference point. For BP, BG, and C0G capacitors of less than 20 pF, the following capacitance change limits shall apply:

Permissible capacitance change from capacitance at +25°C in ppm/°C					
Temperature	Less than 2.1 pF	2.15 pF to 4.2 pF	4.3 pF to 8.0 pF	8.1 pF to 18 pF	Greater than 18 pF
+125°C	1/	±250 ppm/°C	±120 ppm/°C	±60 ppm/°C	±30 ppm/°C
-55°C 2/	1/	+246.25 -326.25	+116.25 -166.25	+55.00 -91.25	+27.50 -53.75

1/ Not practically measurable.
2/ The ppm/°C values for -55°C were calculated by dividing ppm by -80°C.

3.19 Temperature humidity bias. When tested in accordance with 4.6.15, IR shall not be less than 30 percent of the initial +25°C value specified (see 3.8).

3.20 Life (at elevated ambient temperature). When tested in accordance with 4.6.16, capacitors shall meet the following requirements:

a. 250-hour limits:

(1) Insulation resistance (at +125°C): Shall not be less than 50 percent of the value specified (see 3.8).

(2) Visual examination: No mechanical damage. Marking shall remain legible, if applicable.

(3) Insulation resistance (at +25°C): Shall not be less than 50 percent of the value specified (see 3.8).

(4) Capacitance: Change not to exceed ±15 percent from the initial measured value for class II characteristics, and ±0.3 percent or 0.3 pF, whichever is greater, from the initial measured value for class I characteristics.

(5) Dissipation factor: Shall not exceed the limit specified (see table VII).

b. 1,000-hour, 2,000-hour, and 4,000-hour limits:

(1) Insulation resistance (at +125°C): Shall not be less than 30 percent of the value specified (see 3.8).

(2) Visual examination: No mechanical damage. Marking shall remain legible, if applicable.

(3) Insulation resistance (at +25°C): Shall not be less than 30 percent of the value specified (see 3.8).

(4) Capacitance: Change not to exceed ±20 percent from the initial measured value for class II characteristics, and ±0.5 percent or 0.5 pF, whichever is greater, from the initial measured value for class I characteristics.

(5) Dissipation factor:

(a) Class II characteristics: Shall not exceed the limits specified in table XI.

(b) Class I characteristics: Shall not be more than 20% greater than the initial specified limit (see table VII).

TABLE XI. Class II characteristic dissipation factor limits.

Rated Voltage (V_{dc})	Maximum DF (%)
≥ 50V	3.0
16V – 25V	5.0
10V	7.5
4V – 6.3V	10

3.21 Dielectric voltage breakdown. When tested in accordance with 4.6.17, failure shall occur at greater than 6X rated voltage or 1,200 V_{dc}, whichever is less. A failure shall be defined as a steady state current between 150 µA and 5 mA.

3.22 Marking.

3.22.1 Package marking. Packaging containers shall be marked with the PIN (see 1.2.1), capacitance, capacitance tolerance, voltage, "JAN" brand, lot symbol, date code, and the CAGE code. The PIN shall include the electrode material code whether or not it was used for acquisition. Other markings which in any way interfere with, obscure, or confuse those specified herein are prohibited.

3.22.2 Capacitor marking (T Level only). Capacitors size 0805 and larger shall be legibly marked in a contrasting color in accordance with either of the two options below. The capacitor marking shall include the manufacturer's trademark or symbol on case sizes 1210 and larger. Other markings which in any way interfere with, obscure, or confuse those specified herein are prohibited. The marking shall withstand the environmental conditions specified herein. The marking shall be a minimum resistance of 1×10^9 ohms per square and shall remain legible after coating the capacitors with 1.5 to 3 mils of transparent conformal coating such as polyurethane, acrylic, or the equivalent. Capacitor marking is not required for M level product.

a. Option A: In accordance with table XII.

b. Option B: In accordance with table XIII using a two character system. The first character shall be an alphabetic symbol and shall designate the first and second significant figures. The second character shall be a numerical digit and shall designate the decimal multiplier of capacitance in pF (e.g., A1 = 1×10^1 = 10 pF, J5 = 2.2×10^5 = 0.22×10^6 0.22 μF). The marking shall appear in black or legible contrast. The size and orientation of the marking shall be the option of the manufacturer.

Additional marking may appear provided that it does not interfere with the required marking.

3.22.3 Supplying to looser capacitance tolerance and lower rated voltage. Capacitors qualified and marked to tighter capacitance tolerance or higher rated voltage, with acquiring activity approval, are substitutable for capacitors marked to looser capacitance tolerance or lower rated voltage, provided all other values, such as case size, and characteristic, the same. The substitutable capacitors shall not be remarked unless specified in the contract or purchase order (see 6.2), the lot date codes on the capacitors are unchanged, and the workmanship criteria is met.

3.22.4 JAN and J marking. The United States Government has adopted and is exercising legitimate control over the certification marks "JAN" and "J", respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to, and meeting all of the criteria specified herein and in applicable specifications shall bear the certification mark "JAN" except that items too small to bear the certification mark "JAN" shall bear the letter "J". The "JAN" or "J" shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the "JAN" or "J" may be located on the first line above or below the part number. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein or in applicable specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets, the manufacturer shall remove completely the military part number and the "JAN" or the "J" from the sample tested and also from all items represented by the sample. The "JAN" or "J" certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration Number 504,860 for the certification mark "JAN" and Registration Number 2,577,735 for the certification mark "J".

3.23 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.24 Workmanship. Capacitors shall be processed in such a manner as to be uniform in quality when examined under the magnification specified in appendix B.

TABLE XII. Marking for capacitors.

Character	Significant units	Capacitance (pF) and multiplier					
		Orange (x 0.1)	Black (x 1.0)	Green (x 10)	Blue (x 100)	Violet (x 1000)	Red (x 10,000)
A	10	1.0	10	100	1000	10,000	100,000
B	11	1.1	11	110	1100	11,000	110,000
C	12	1.2	12	120	1200	12,000	120,000
D	13	1.3	13	130	1300	13,000	130,000
E	15	1.5	15	150	1500	15,000	150,000
H	16	1.6	16	160	1600	16,000	160,000
I	18	1.8	18	180	1800	18,000	180,000
J	20	2.0	20	200	2000	20,000	200,000
K	22	2.2	22	220	2200	22,000	220,000
L	24	2.4	24	240	2400	24,000	240,000
N	27	2.7	27	270	2700	27,000	270,000
O	30	3.0	30	300	3000	30,000	300,000
R	33	3.3	33	330	3300	33,000	330,000
S	36	3.6	36	360	3600	36,000	360,000
T	39	3.9	39	390	3900	39,000	390,000
V	43	4.3	43	430	4300	43,000	430,000
W	47	4.7	47	470	4700	47,000	470,000
X	51	5.1	51	510	5100	51,000	510,000
Y	56	5.6	56	560	5600	56,000	560,000
Z	62	6.2	62	620	6200	62,000	620,000
3	68	6.8	68	680	6800	68,000	680,000
4	75	7.5	75	750	7500	75,000	750,000
7	82	8.2	82	820	8200	82,000	820,000
9	91	9.1	91	910	9100	91,000	910,000

TABLE XIII Optional marking for capacitors.

First character				Second character	
Alphabetic character	Significant figures	Alphabetic character	Significant figures	Numerical character	Decimal multiplier
A	1.0	T	5.1	0	10^0
B	1.1	U	5.6	1	10^1
C	1.2	V	6.2	2	10^2
D	1.3	W	6.8	3	10^3
E	1.5	X	7.5	4	10^4
F	1.6	Y	8.2	5	10^5
G	1.8	Z	9.1	6	10^6
H	2.0	a	2.5	7	10^7
J	2.2	b	3.5	8	10^8
K	2.4	d	4.0	9	10^9
L	2.7	e	4.5		
M	3.0	f	5.0		
N	3.3	m	6.0		
P	3.6	n	7.0		
Q	3.9	t	8.0		
R	4.3	y	9.0		
S	4.7				

4. VERIFICATION

4.1 Classification of inspections. The inspections specified herein are classified as follows:

a. Qualification inspection (see 4.4).

b. Verification of qualification (see 4.4.4).

c. In-process inspection (T level only, see 4.5.1).

d. Conformance inspection (T level: see 4.5.2.2 and 4.5.2.3. M level: see 4.5.2.2).

e. Periodic inspection (T level: see 4.5.3. M level: see 4.5.2.3 and 4.5.3)

4.2 QPL system. The manufacturer shall establish and maintain a QPL system in accordance with 3.3. Evidence of such compliance is a prerequisite for qualification and retention of qualification.

4.2.1 Purchased raw materials. The following documentation for purchased raw materials shall be retained:

a. Procurement documentation: Traceability.

b. Physical and chemical property data.

c. Performance evaluation/characterization data, if applicable.

4.2.2 In-house prepared materials. The following documentation for in-house prepared materials shall be retained:

a. Fabrication process control data.

b. Physical and chemical property data.

c. Performance evaluation/characterization data, if applicable.

4.2.3 Manufacturing lot performance information. Lot performance information relating to material, process, lot conformance, inspections, and product shall be retained by the manufacturer for 10 years from the date of the manufacture of the capacitors.

4.3 Inspection conditions and reference measurements.

4.3.1 Conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the “GENERAL REQUIREMENTS” of MIL-STD-202, except relative humidity shall not exceed 75 percent. Accuracy of all test voltage measurements shall be within ±2.0 percent of the specified voltage. Unless otherwise specified herein, all test temperatures above +25°C shall have a tolerance of +4°C, -0°C.

4.3.2 Reference measurements. When requirements are based on comparative measurements made before and after conditioning, the reference measurement shall be considered the last measurement made at +25°C ±3°C prior to conditioning. Unless reference measurements have been made within 30 days prior to the beginning of conditioning, they shall be repeated.

4.3.3 Power supply. The power supply used for life testing shall have a regulation of ±2 percent or less of the specified test voltage.

4.3.4 Manufacturer's production inspection. The manufacturer may perform tests equal to or more stringent than those specified in in this document if approved by the qualifying activity. The following criteria shall be complied with:

a. Tests conducted by the manufacturer during production shall be clearly identical to or more stringent than that specified. (NOTE: Includes optional voltage conditioning (see 4.6.3.2.3)).

b. The parameters measured and the failure criteria shall be the same or more stringent than those specified herein.

c. The lot rejection criteria is the same or more stringent than that specified herein.

d. Once approved, the manufacturer shall not change the test procedures or criteria without prior notification and concurrence by the qualifying activity.

4.3.5 Mounting. When specified in the test procedure, the chip capacitor shall be mounted on an FR4 or ceramic substrate board. The test board material shall be such that it shall not be the cause of, nor contribute to, any failure of a chip capacitor in any of the tests for which it may be used. A test board shall be prepared with metallized surface land areas of proper spacing to permit mounting of chips by soldering the terminations of the chips to the test board land areas. Unless otherwise specified, the dimensions of the test card are optional. The metallization material shall be compatible with the bonding technique to be employed and the material used on the chip termination. The method of chip mounting for the different termination materials shall be as follows:

a. Terminations D, R, and Z (solderable). Capacitors shall be mounted on a test board by soldering the chip terminations directly to the test board metallized land areas in accordance with the following:

(1) Solder and soldering flux shall be of such a quality as to enable the chip capacitors to meet all the requirements of this specification and shall be applied to the terminations of each capacitor.

(2) All capacitors shall be placed across the metallized land areas of the test board with contact between the capacitors terminations and board land areas only. The use of adhesive to keep capacitors in place during mounting operation is allowable.

(3) Only ambient air cooling shall be used.

b. Termination M (palladium/silver alloy). Capacitors shall be attached to the substrate with a conductive adhesive. The conductive adhesive shall be cured at a minimum temperature of +150°C. The minimum curing time shall be 30 minutes.

c. Terminations G and V (gold). Capacitors may be mechanically attached to the substrate with a non-conductive adhesive. The capacitors shall then be electrically connected using wire bonds between the termination and the test board metalized lands. Alternately, capacitors may be attached to the substrate with a conductive adhesive. The conductive adhesive shall be cured at a minimum temperature of +150°C. The minimum curing time shall be 30 minutes.

4.3.6 Post-test visual examinations. When a post-test visual examination is required, capacitors shall be examined under the magnification specified in appendix B.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the qualifying activity (see 6.3) on sample units produced with equipment and procedures normally used in production.

4.4.1 Sample size. The number of capacitors to be specified for qualification inspection shall be in accordance with table XIV and in appendix A of this specification.

4.4.2 Test routine. Sample units shall be subjected to the qualification inspection specified in table XIV in the order shown. T level sample units shall have been subjected to the in-process screening required by this specification. All sample units shall be subjected to the inspection of group I. The sample shall then be divided in accordance with table XIV as applicable.

4.4.3 Failures. Failures in excess of those allowed in table XIV shall be cause for refusal to grant qualification approval.

TABLE XIV. Qualification inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of sample units to be inspected	Number of failures allowed 1/
Group I (Screening)				
Thermal shock and voltage conditioning	3.7	4.6.3	254 min 2/	See table XVII
Insulation resistance (at +125°C)	3.8	4.6.4		
Dielectric withstanding voltage	3.9	4.6.5		
Insulation resistance (at +25°C)	3.8	4.6.4		
Capacitance	3.10	4.6.6		
Dissipation factor	3.11	4.6.7		
Group II				
Visual and mechanical examination; material, physical dimensions, design, construction, marking, and workmanship	3.1, 3.4, 3.22 and 3.24	4.6.2	15	1
Destructive physical analysis	3.12	4.6.8		
Group IIIa				
Board flex	3.13	4.6.9	18 4/	0
Shear stress	3.14	4.6.10		
Group IIIb				
Solderability (terminations D, R, and Z only)	3.15	4.6.11	12	0
Bond strength (wire) (terminations G and V only)	3.16	4.6.12		
Group IIIc				
Resistance to soldering heat	3.17	4.6.13	22	0
Group IVa 3/				
Voltage-temperature limits / temperature characteristic	3.18	4.6.14	12	0
Group IVb 3/				
Temperature humidity bias	3.19	4.6.15	22	0
Group V				
Thermal shock	3.7	4.6.3	123	1
Life	3.20	4.6.16		
Group VI				
Dielectric voltage breakdown	3.21	4.6.17	30	0

1/ A sample unit having one or more defects will be charged as a single defective.
2/ Additional samples over the 254 minimum should be included, based on table XVII, to allow for the percent defective allowable.
3/ Leads may be soldered to chip capacitor to facilitate the tests required in group IV.
4/ The samples shall be divided evenly for the board flex and shear stress tests.

4.4.4 Verification of qualification. Every 12 months, the manufacturer shall provide verification of qualification to the qualifying activity. Continuation of qualification shall be based on meeting the following requirements:

a. MIL-STD-790 program.

b. Product design has not been modified.

c. Certification that the manufacturer still maintains the capabilities and facilities necessary to produce these items.

d. Verification of the results of group A, group B, and group C inspections including identification of failed lots and subgroups and failure modes.

4.5 In-process inspection and quality conformance inspection.

4.5.1 In-process inspection. Each production lot of T level capacitors shall be inspected in accordance with table XV. Other screening examinations may be applied at the option of the manufacturer, as approved by the qualifying activity.

TABLE XV. In-process inspection.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure
Ultrasonic inspection (pre-termination)	3.5	4.6.1	100%
Visual examination (post termination)	3.6	4.6.2	100%

4.5.1.1 Rework. Rework is not allowed on any operations including and subsequent to the formation of the slurry, except for marking.

4.5.2 Inspection of product for delivery. Inspection of M level product for delivery shall consist of group A inspection. Inspection of T level product of product for delivery shall consist of in-process inspection, group A, and group B inspection.

4.5.2.1 Production and Inspection lot.

4.5.2.1.1 Production lot. A production lot shall consist of all capacitors of a single nominal capacitance/voltage rating of one design, from the same dielectric material lot, and processed as a single lot through all manufacturing steps on the same equipment. The lot may contain all available capacitance tolerances for the nominal capacitance value. In addition, the lot shall conform to the following:

a. For T level product, raw materials, such as end terminations, solder, ceramic raw material, binders, and electrode ink, shall be traceable to the same material lot and be from the same contractor.

b. For T level product, a lot number shall be assigned before electrode printing (inking) and be manufactured from the same slurry and cast on the same belt or comparable equipment (see 3.4).

c. For T level product, a single mix of a basic ceramic formulation fired through one kiln with one temperature profile during the process, with constant dielectric design, with, in general, no more than 20 percent variation in the number of active dielectrics being assembled in one continuous buildup. Sublots may be allowed to provide a spread in capacitance value to improve the yield. This will normally be done in the case of tight tolerances and low capacitance. In some cases, more than 20 percent variation in the number of active dielectrics may be required in these circumstances (see 3.3).

d. For T level product, end termination material shall be consistent in formulation and traceable to a single material lot and shall be fired in the same kiln with one temperature profile during the process. All capacitors shall enter the kiln in one continuous operation/run for end termination firing.

e. Lot identity shall be maintained from the time the lot is assembled to the time it is accepted.

f. The lot date code shall be assigned prior to the start of group A.

g. The manufacturer may manufacture and test the production lot based on the voltage rating for that design and subsequently supply the final product at any voltage rating equal to or less than that for which it was manufactured and tested.

4.5.2.1.2 Inspection lot. An inspection lot shall consist of all capacitors of the same dielectric classification (class I or class II (see table I)), produced under essentially the same conditions with the same basic materials, and offered for inspection at one time. Samples selected from the inspection lot shall be representative of the capacitance values and voltages in the approximate ratio of production.

4.5.2.2 Group A inspection. Group A inspection shall consist of the tests and examinations specified in table XVI. The following details shall apply:

a. Failure to meet percent defectives allowable (PDA) limits shall cause the lot to be rejected.

b. For T level product, a summary of the results of group A inspection on each lot that meets requirements shall be submitted to the purchaser with the capacitors.

c. For T level product, a copy of the applicable DPA report shall be submitted to the purchaser with each lot of capacitors.

TABLE XVI. Group A inspection.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure
Subgroup 1			
Thermal shock (T level only)	3.7	4.6.3	
Ultrasonic inspection (T level sizes ≥ 0805 only)	3.5	4.6.1	100% inspection (see table XVII)
Voltage conditioning 1/ 2/	3.7	4.6.3	
Subgroup 2			
Visual and mechanical inspection; material, physical dimensions, design, construction, marking, and workmanship	3.1, 3.4, 3.22, and 3.24	4.6.2	20 samples 0 failures
Subgroup 3			
Destructive physical analysis (T level only)	3.12	4.6.8	See table XVIII
Subgroup 4			
Solderability (terminations D, R, and Z only)	3.15	4.6.11	5/0
Bond strength (wire) (terminations G and V only)	3.16	4.6.12	5/0 (10 wires)
Shear stress (termination M only)	3.14	4.6.10	5/0

1/ The DWV post-test is not applicable if optional voltage conditioning was performed at 250 percent or more of the rated voltage.
2/ Capacitance and dissipation factor failures shall be removed from the lot but shall not be considered defective for the determination of the percent defective allowed (see 4.5.2.2.1.1 and table XVII).

4.5.2.2.1 Subgroup 1.

4.5.2.2.1.1 Sampling plan. Subgroup 1 tests shall be performed on a production lot basis on 100 percent of the product supplied under this specification. Capacitors failing the tests of subgroup 1 shall be removed from the lot. If screening requires more than the percent defectives allowable (PDA) in table XVII, the entire lot shall be rejected.

4.5.2.2.1.2 Rejected lots. Rejected T level lots shall not be supplied to this specification; however, they may be supplied as M level product provided they meet all of the M level requirements. For M level product, production lots exceeding 8 percent defective allowable (see table XVII) shall be segregated from new lots that have passed inspection. Rejected lots may be offered for acceptance only if the manufacturer 100 percent retests to the requirements of subgroup 1. Resubmitted lots shall be kept separate and shall be clearly identified as resubmitted lots. If, during 100 percent reinspection to subgroup 1, the lot exceeds 3 percent defective, the lot shall be rejected and shall not be supplied to this specification.

TABLE XVII. Percent defectives allowable for qualification (group I) and group A (subgroup 1).

Product level	PDA for last 48 hours during voltage conditioning at +125°C 1/	PDA overall 2/ (%)
T	1 unit or 0.2 percent, whichever is greater	5
M	N/A	8

1/ For optional voltage conditioning, the time required for meeting the PDA shall be calculated with the $T_{test(PDA)}$ equation in 4.6.3.2.3.
2/ Overall PDA applies to voltage conditioning only.

4.5.2.2.2 Subgroup 2.

4.5.2.2.2.1 Sampling plan. Subgroup 2 tests shall be performed on an inspection lot basis for M level product and a production lot basis for T level product. In the event of one or more failures, the lot shall be rejected.

4.5.2.2.2.2 Rejected lots. Rejected T level lots shall not be supplied to this specification; however, they may be supplied as M level product provided they meet all of the M level requirements. For M level product, the rejected lot shall be segregated from new lots and those that have passed inspection. The rejected lot shall be 100 percent inspected for those quality characteristics found defective in the sample and any defectives found removed from the lot. A new sample of capacitors shall then be randomly selected in accordance with table XVI. If one or more defects are found in this second sample, the production lot shall be rejected and shall not be supplied to this specification.

4.5.2.2.3 Subgroup 3 (T level only).

4.5.2.2.3.1 Sampling plan. Samples shall be selected randomly from every T level production lot in accordance with table XVIII and subjected to the DPA test. The accept/reject criteria shall be in accordance with table XVIII.

4.5.2.2.3.2 Rejected lots. Rejected lots shall not be supplied to this specification; however, they may be supplied as M level product provided they meet all of the M level requirements.

TABLE XVIII. Destructive physical analysis sample size.

Lot size	Minimum sample size	Accept	Reject
1 - 500	14	0	1
501 - 10,000	32	1	2
10,001 - 35,000	50	2	3
35,001 - 500,000	80	3	4

4.5.2.2.4 Subgroup 4.

4.5.2.2.4.1 Sampling plan. Subgroup 4 tests shall be performed on an inspection lot basis for M level capacitors and on a production lot basis for T level capacitors. The samples shall be selected randomly and subjected to the subgroup 4 tests. The manufacturer may use electrical rejects from the subgroup 1 and subgroup 2 tests for all or part of the samples to be used for subgroup 4 testing. If there are one or more defects, the lot shall be rejected.

4.5.2.2.4.2 Rejected lots. Rejected T level lots shall not be supplied to this specification. If inspection lot sampling is used for M level product, each production lot used to form the rejected inspection lot shall be individually submitted to subgroup 4 testing as specified in 4.5.2.2.4.1. Rejected M level production lots shall not be supplied to this specification.

4.5.2.2.4.3 Disposition of samples. The subgroup 4 tests are considered destructive and samples submitted to the subgroup 4 tests shall not be supplied on the contract or order.

4.5.2.3 Group B inspection. Group B inspection shall consist of the tests specified in table XIX and shall be performed on sample units from lots that have been subjected to and have passed group A inspection. For T level, group B shall be performed on a production lot basis. Copies of group B read and record data shall be forwarded to purchaser with T level capacitors. T level capacitors may not be shipped until the conclusion of 1,000 hours of life test. For M level, group B shall be performed on an inspection lot basis every 6 months. Except where the results of this inspection show noncompliance with the applicable requirements (see 4.5.2.3.3), delivery of M level capacitors which have passed group A inspection shall not be delayed pending the results of this inspection.

TABLE XIX. Group B inspection.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure	Accept/ Reject
Subgroup 1 Thermal shock Life	 3.7 3.20	 4.6.3 4.6.16	 Table XX (T level) Table XXI (M level)	 Table XX (T level) Table XXI (M level)
Subgroup 2 Temperature humidity bias (at rated voltage)	3.19	4.6.15	12	0
Subgroup 3 Voltage-temperature limits / temperature characteristic	3.18	4.6.14	12	1
Subgroup 4 Dielectric voltage breakdown	3.21	4.6.17	12	0

4.5.2.3.1 Sampling plan.

4.5.2.3.1.1 Subgroup 1. The number of samples required by table XX shall be selected from each T level production lot. For M level product, the number of sample units required by table XX shall be selected from production every 6 months. Four groups shall be formed, as applicable (see below). Testing shall only be required for groups produced during the 6 month period.

Group 1 - Chip sizes smaller than 0805 (/1, /2, and /3). Group 1 shall be divided into two dielectric classification groups (class I and class II (see table I)) as shown in table XXI. Capacitor sizes manufactured during the period shall be represented, as far as practical, in the approximate ratio of production for each dielectric classification. The highest capacitance value in the largest chip size produced in each of the two dielectric classifications shall be represented in the sample. If only one dielectric classification is produced during the period, all samples shall be of that dielectric classification; however, the total number of samples (32) shall remain unchanged.

Group 2 - Chip sizes 0805 and larger (/4, /5, /6, /7, and /8). Group 2 shall be divided into two dielectric classification groups (class I and class II (see table I)) as shown in table XXI. Capacitor sizes manufactured during the period shall be represented, as far as practical, in the approximate ratio of production for each dielectric classification. The highest capacitance value in the largest chip size produced in each of the two dielectric classifications shall be represented in the sample. If only one dielectric classification is produced during the period, all samples shall be of that dielectric classification; however, the total number of samples (32) shall remain unchanged.

Group 3 - Chip sizes 0306 (/9) and 0508 (/10). Capacitor sizes manufactured during the period shall be represented, as far as practical, in the approximate ratio of production. The highest capacitance value in the largest case size produced during the period shall be included in the sample.

Group 4 - Interdigitated capacitors (IDC) (/11, /12, and /13). Capacitor sizes manufactured during the period shall be represented, as far as practical, in the approximate ratio of production. The highest capacitance value in the largest case size produced during the period shall be included in the sample.

TABLE XX. T level group B, subgroup 1 sampling plan.

Lot Size	Minimum Sample Size	1000 Hours	
		Accept	Reject
1-3200	32	0	1
3201+	125	1	2

TABLE XXI. M level group B, subgroup 1 sampling plan. 1/

Group 1		Group 2		Group 3	Group 4
class I	class II	class I	class II	32	32
16	16	16	16		

1/ No failures allowed.

4.5.2.3.1.2 Subgroup 2 through subgroup 4. The number of samples required by table XIX shall be taken from each T level production lot. For M level product, the number of samples required by table XIX of each dielectric classification (class I and class II (see table I)) shall be randomly selected from inspection lots every 6 months.

If a manufacturer can demonstrate that the subgroup 3 test has been performed five consecutive times with zero failures, the frequency of this test, with the approval of the qualifying activity, can be performed on an annual basis. If the design, material, construction, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency.

4.5.2.3.2 Disposition of sample units. Sample units that have been subjected to group B inspection shall not be delivered on the contract.

4.5.2.3.3 Noncompliance (M level only). If a sample unit fails to pass group B inspection, the manufacturer shall notify the qualifying activity and cognizant inspection activity of such failure and take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials and processes, and which are considered subject to the same failure. Acceptance and shipment of the product shall be discontinued until corrective action, acceptable to the Government, has been taken. After the corrective action has been taken, group B inspection shall be repeated on additional sample units (all inspections), or the inspection that the original sample failed, at the option of the qualifying activity. Group A inspection may be reinstituted, however, final acceptance shall be withheld until the group B inspection has shown that corrective action was successful. In the event of failure after reinspection, information concerning the failure and corrective action taken shall be furnished to the cognizant inspection activity and the qualifying activity.

4.5.3 Group C inspection. Group C inspection shall consist of the tests specified in table XXII in the order shown. Samples shall be randomly selected from inspection lots that have passed the group A inspection every 3 months. Delivery of products that have passed group A inspections shall not be delayed pending the results of group C inspection.

4.5.3.1 Disposition of sample units. Sample units that have been subjected to groups B and C inspections shall not be delivered on the contract. T level samples shall be maintained by the manufacturer for a minimum of 10 years.

4.5.3.2 Noncompliance. If a sample fails to pass group C inspection, the manufacturer shall notify the qualifying activity and the cognizant inspection activity of such failure and take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials and processes, and which are considered subject to the same failure. Acceptance and shipment of the product shall be discontinued until corrective action, acceptable to the Government, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspection) or the inspection which the original sample failed, at the option of the qualifying activity. Group A (and group B if applicable) inspection may be reinstituted; however, final acceptance shall be withheld until the group C inspection has shown that corrective action was successful. In the event of failure after re-inspection, information concerning the failure and corrective action taken shall be furnished to the cognizant inspection activity and the qualifying activity.

TABLE XXII. Group C inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of units to be inspected	Number of defectives permitted
Subgroup 1				
Board flex	3.13	4.6.9	12 1/	0
Shear stress	3.14	4.6.10		
Subgroup 2				
Resistance to soldering heat	3.17	4.6.13	6	0

1/ The samples shall be divided evenly for the board flex and shear stress tests.

4.6 Methods of inspection.

4.6.1 Ultrasonic inspection (see 3.5). Capacitors shall be examined in accordance with appendix C. The following details and exceptions shall apply:

a. Output device. Either a hard or soft copy shall be acceptable provided defects are noted on the copy. Soft copies shall be in non-proprietary software format.

b. Views. Views shall be bulk scan.

c. Scan resolution. Scan resolution shall be .005 inch or less. Capacitors greater than .055 inch thick shall be imaged double-sided. At the option of the manufacturer, capacitors less than .055 inch thick may be imaged double-sided.

d. Retention. Retention shall be in accordance with 4.2.3.

4.6.2 Visual examination (see 3.6). Capacitors shall be examined under magnification in accordance with appendix B and shall meet the visual requirements of appendix B.

4.6.3 Thermal shock and voltage conditioning (see 3.7). Capacitors shall be subjected to the tests of 4.6.3.1 and 4.6.3.2, as applicable (see table XIV, table XVI, and table XIX).

4.6.3.1 Thermal shock. Capacitors shall be tested in accordance with method 107 of MIL-STD-202. The following details shall apply:

a. Test condition A, except that in step 3, sample units shall be tested at +125°C.

b. Number of cycles:

(1) Qualification:

(a) T level: 100 cycles.

(b) M level: 20 cycles.

(2) Group A (T level only): 20 cycles.

(3) Group B:

(a) T level: 100 cycles.

(b) M level: 5 cycles.

c. Mounting:

(1) Qualification and group B: Capacitors shall be mounted in accordance with 4.3.5 on FR4 printed circuit board (PCB). At the option of the manufacturer, all termination styles may be solder mounted.

(2) Group A: Not applicable.

4.6.3.2 Voltage conditioning (see 3.7). Capacitors shall be subjected to the voltage conditioning test in 4.6.3.2.1 for T level or 4.6.3.2.2 for M level or the optional voltage conditioning test in 4.6.3.2.3. It shall be verifiable that all capacitors offered for electrical tests have been exposed to the required voltage conditioning for the required time duration. When the optional voltage conditioning test of 4.6.3.2.3 is used, the traveler shall include the specific accelerated voltage used and the test duration. See figure 4 for a suggested test circuit. An alternate test circuit can be used, provided the notes of figure 4 are followed.

4.6.3.2.1 T level standard voltage conditioning (see 3.7). Standard voltage conditioning shall be started after completion of the thermal shock test. The voltage conditioning shall consist of applying twice the rated voltage to the units at the maximum rated temperature of +125°C +4°C, -0°C for a minimum of 168 hours and a maximum of 264 hours. Voltage conditioning may be terminated at any time during the 168 to 264 hour time interval, provided that the number of failures detected during the last 48 hours of test meets the PDA requirements specified in table XVII. Failures shall be determined by blown fuses or hot IR failures. Voltage shall be applied and shall reach maximum value within 2 minutes, maximum. After completion of the exposure period, the following electrical measurements shall be performed:

a. Insulation resistance (+125°C): In accordance with 4.6.4. Note: This step may be skipped if step c is done at +125°C with +25°C test limits.

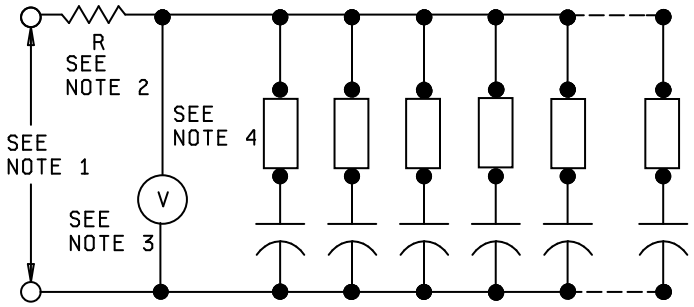
b. Dielectric withstanding voltage: In accordance with 4.6.5.

c. Insulation resistance (+25°C): In accordance with 4.6.4.

d. Capacitance: In accordance with 4.6.6.

e. Dissipation factor: In accordance with with 4.6.7.

The manufacturer has the option of performing these electrical tests in any order except insulation resistance shall always be done after dielectric withstanding voltage. If the voltage conditioning test is performed with individual fuses in series with each capacitor, any capacitor tested in a position where a fuse fails shall be tested for insulation resistance and dielectric withstanding voltage. If the capacitor meets the initial requirements for insulation resistance and dielectric withstanding voltage, the capacitor shall be rejected but shall not count against the PDA in table XVII. The manufacturer also has the option to not test capacitors with fuse failures and count these toward the PDA.



NOTES:
1. The power supply shall be capable of supplying the required test voltage.
2. The current limiting device shall be a resistor and/or a fuse. The current shall be limited to no more than 10 A.
3. There shall be a voltage monitor that will trigger an alarm and shut off the test if the applied voltage drops by more than 5 percent. Time without voltage does not apply toward the minimum voltage conditioning hours (see 4.6.3.2.1 and 4.6.3.2.2).
4. At the option of the manufacturer, a fuse or a resistor may be used in series with each capacitor. The value of the resistors and fuses shall be such that they do not restrict the power supply's ability to provide the required test voltage to the capacitor under test (±5 percent).

FIGURE 4. Voltage conditioning circuitry.

4.6.3.2.2 M level Standard voltage conditioning (see 3.7). A minimum of twice the rated voltage shall be applied to the capacitors at the maximum rated temperature +4°C, -0°C for 100 hours +25 hours, -4 hours. After completion of the exposure period, the units shall be stabilized at room temperature and the DWV, IR, capacitance, and DF shall be measured in accordance with 4.6.5, 4.6.4, 4.6.6, and 4.6.7, respectively.

4.6.3.2.3 Optional voltage conditioning (see 3.7). The manufacturer, with approval from the qualifying activity, may perform an optional voltage conditioning test instead of the standard voltage conditioning tests of 4.6.3.2.1 and 4.6.3.2.2. All conditions of 4.6.3.2.1 and 4.6.3.2.2 apply, with the exception of the voltage applied, the test time, and the time required for meeting the PDA (T level only). The accelerated condition selected for the optional voltage conditioning shall be used for the duration of the test. At no time shall a combination of standard and optional voltage conditioning be allowed on the same samples. The minimum time duration, $T_{test(min.)}$, and the time required for meeting the PDA, $T_{test(PDA)}$, shall be calculated as follows:

$$T_{test(min.)} = \frac{A}{(E_{test}/E_{rated})^3} \qquad T_{test(PDA)} = \frac{384}{(E_{test}/E_{rated})^3}$$

Where: $2 \times E_{rated} \leq E_{test} \leq 4 \times E_{rated}$

E_{test}	=	Applied voltage
E_{rated}	=	Rated voltage of the capacitor
$T_{test(min.)}$	=	Minimum test time in hours
$T_{test(PDA)}$	=	Time required for meeting the PDA (T level only)
A	=	1344 for T level or 800 for M level based on an assumed acceleration factor of 8:1.

4.6.4 Insulation resistance (see 3.8). Capacitors shall be tested in accordance with method 302 of MIL-STD- 202. The following details shall apply:

a. Test potential: Rated voltage (see 3.1).

b. Special conditions: If a failure occurs at a relative humidity above 50 percent, the insulation resistance may be measured again at any relative humidity less than 50 percent.

c. Points of measurement: Between the mutually insulated points.

4.6.5 Dielectric withstanding voltage (see 3.9). Capacitors shall be tested in accordance with method 301 of MIL-STD-202. The following details shall apply:

a. Magnitude and nature of test voltage: 250 percent to 400 percent of the direct current rated voltage (see 3.1).

b. Duration of application of test voltage: 5 ±1 seconds. The test voltage shall be raised from 0 to the specified value within 1 second, maximum.

c. Points of application of test voltage: Between the capacitor-element terminals.

d. Limiting value of surge current: Shall be limited between 30 and 50 milliamperes.

e. Examination after test: Capacitors shall be examined for evidence of damage and breakdown.

4.6.6 Capacitance (see 3.10). Capacitors shall be tested in accordance with method 305 of MIL-STD-202. The following details and exceptions shall apply:

a. Test frequency:

Test frequency	Characteristic	
	Class I	Class II
1 MHz ±100 kHz 1 kHz ±100 Hz 120 Hz ±10 Hz	< 1,000 pF ≥ 1,000 pF N/A	< 100 pF ≥ 100 pF and ≤ 10 µF >10 µF

b. Voltage: A root-mean-square potential of 1.0 ±0.2 volt for 1MHz and 1kHz and 0.5 ±0.1 volt for 120Hz.

4.6.7 Dissipation factor (see 3.11). The dissipation factor shall be measured with a capacitance bridge or other suitable method at the frequency and voltage specified in 4.6.6. Unless otherwise specified, the inherent accuracy of the measurement shall be ±2 percent of the reading plus 0.1 percent dissipation factor (absolute). Suitable measurement techniques shall be used to minimize errors due to the connections between the measuring apparatus and the capacitor.

4.6.8 Destructive physical analysis (see 3.12). Capacitors shall be examined in accordance with ECIA EIA/ECA-469. The following details shall apply:

a. Sectioning of cast samples: After sectioning in accordance with ECIA EIA/ECA-469, the following is recommended to accurately detect feature size:

(1) After finishing with grit 600, move to 800, then 1000, then 1200, and finally 2400 grit or finer before the final polish with sub-micron diamond (0.3 micron or smaller) or alumina powder and a short/low nap cloth.

(2) Low pressure should be used during grinding.

(3) Plenty of water flow should be used.

(4) A minimal amount of time should be spent on the final polish.

b. Recommended illumination techniques: Use of either vicinal illumination (see 6.9), dark-field illumination with a polarizer, or other techniques approved by the qualifying activity is recommended for inspection for cracks in the ceramic.

4.6.9 Board flex (see 3.13). Capacitors shall be tested for board flex in accordance with the following:

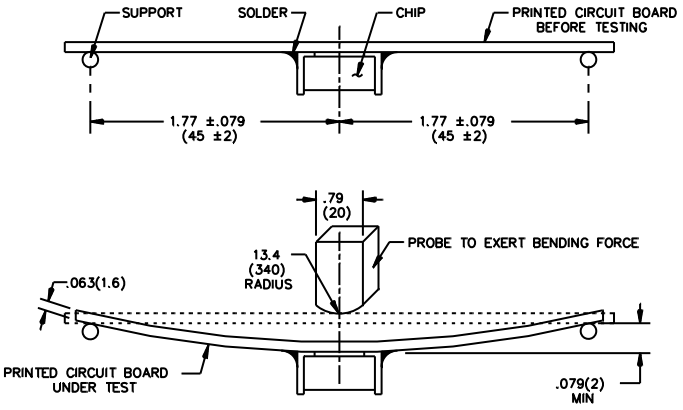
a. Mounting: Capacitors shall be mounted in accordance with 4.3.5 on a 3.94 inches (100 mm) ± .079 inch (2.0 mm) X 1.57 inches (40 mm) ± .079 inch (2.0 mm) FR4 PCB, which is .063 inch (1.6 mm) ± .008 inch (0.20 mm) thick.

b. Procedure: The FR4 PCB shall be placed into a fixture similar to the one shown in figure 5 with the component facing down. A force shall be applied which will bend the board .079 inch (2.0 mm), minimum.

c. Duration of force: The force shall be applied for 60 seconds -0, + 5 seconds.

d. Measurement during test: Capacitance in accordance with 4.6.6.

e. Examinations and measurements after test: Capacitors shall be visually inspected for mechanical damage to the capacitor body, terminals, and body/terminal junction (see 4.3.6). Capacitance and dissipation factor shall then be measured in accordance with 4.6.6 and 4.6.7.



NOTES:
1. Measurements are in inches. Metric equivalents in millimeters are in parentheses and given for general information only.

FIGURE 5. Board flex.

4.6.10 Shear stress (see 3.14). Capacitors shall be tested for shear stress in accordance with the following:

a. Mounting: Capacitors shall be mounted in accordance with 4.3.5. Epoxy adhesives, if applicable, shall be limited to the terminations only.

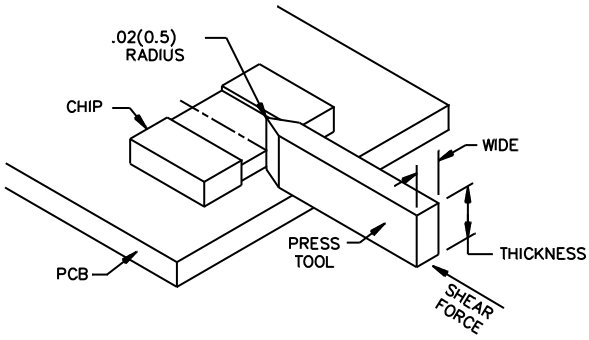
b. Procedure: With the capacitor mounted on a PCB, apply the specified force to the side of the capacitor being tested (see figure 6). The force shall be applied gradually as not to apply a shock to the capacitor being tested.

c. Duration of force: The force shall be applied for 60 seconds ± 1 second.

d. Magnitude of force applied:

Chip Size	Force (Kg)
> 1210	1.8
≥ 0603 and ≤ 1210	1.0
> 0201 and < 0603	0.5
≤ 0201	0.1

e. Examination after test: Capacitors shall be visually inspected for mechanical damage to the capacitor body, terminals, and body/terminal junction (see 4.3.6).



NOTES:
1. Measurements are in inches. Metric equivalents in millimeters are in parentheses and given for general information only.

FIGURE 6. Shear stress.

4.6.11 Solderability (see 3.15). Capacitors shall be tested for solderability in accordance with method 208 of MIL-STD-202. The following details and exceptions shall apply:

a. Each capacitor shall be immersed in molten solder.

b. Number of terminations to be tested: Two.

c. Examination of terminations: Capacitor terminations shall be visually examined for a smooth solder coating and the presence of pinholes or exposed termination material (see 4.3.6). In case of dispute, the percent coverage with pinholes or exposed termination material shall be determined by actual measurement in these areas, as compared to the total area.

4.6.12 Bond strength (wire) (see 3.16). Capacitors shall be tested in accordance with method 2011 of MIL-STD-883. The following details shall apply:

a. Mounting: Capacitors shall be mounted in accordance with 4.3.5.

b. Test condition: D.

4.6.13 Resistance to soldering heat (see 3.17). Capacitors shall be tested in accordance with method 210 of MIL-STD-202. The following details and exceptions shall apply:

a. Mounting: Capacitors shall be mounted in accordance with 4.3.5.

b. Test condition: J, except with only one heat cycle.

c. Measurements after test: After completion of the cleaning process and following a minimum 10-minute to maximum 24-hour cooling period, the IR, capacitance, and DF shall be measured in accordance with 4.6.4, 4.6.6, and 4.6.7, respectively.

d. Examination after test: Capacitors shall be visually examined for evidence of mechanical damage (see 4.3.6).

4.6.14 Voltage-temperature limits / temperature characteristic (see 3.18). The temperature of each capacitor shall be varied in accordance with table XXIII. Capacitance measurements shall be made at the frequency and voltage specified in 4.6.6. The percentage of dc rated voltage (see table I) need only be applied to the capacitor in each of step E through step G inclusive (not applicable to C0G, X7R, and X7S), until voltage stability is reached and the capacitance measurement is made. Capacitance measurements shall be made at each step specified in table XXIII and at a sufficient number of intermediate points between step B and step G to establish a true characteristic curve. Capacitance measurements at each temperature shall be taken only after the test temperature has stabilized.

4.6.14.1 Voltage-temperature limits / temperature characteristic for quality conformance inspection. Capacitance measurements shall be made in accordance with 4.6.6, except that the measurements shall be made only for steps C, D, E, and G of table XXIII for characteristics BG, BP, BR, BX, BZ, and BN. Measurements shall be made for steps A through D for C0G, X7R, and X7S.

TABLE XXIII. Voltage-temperature limit / temperature characteristic cycle.

Step	Voltage (dc)	Temperature (°C)
A	None	+25 ± 2
B	None	-55 ± 2
C 1/	None	+25 ± 2
D	None	+125 ± 2
E	see table I	+125 ± 2
F	see table I	+25 ± 2
G	see table I	-55 ± 2

1/ Reference point.

4.6.15 Temperature humidity bias (see 3.19). Capacitors shall be tested in accordance with the following:

a. Mounting: Capacitors shall be mounted in accordance with 4.3.5. At the option of the manufacturer, all termination styles may be solder mounted.

b. Procedure: Capacitors shall be subjected to an environment of +85°C with 85 percent relative humidity. A dc potential of rated voltage (+/- 5 percent) shall be applied continuously.

c. Duration:

(1) Qualification: 1000 hours, minimum.

(2) Group B: 96 hours, minimum.

c. Test circuit: There shall be one series resistor for each capacitor under test. The value of the series resistor shall be such that there is not greater than 5% voltage drop across the resistor as long as the IR value of the capacitor meets the IR specification.

d. Measurements after test: Capacitors shall be removed from the chamber and allowed 3 hours ±30 minutes to dry and stabilize at +25°C. IR shall then be measured in accordance with 4.6.4.

4.6.16 Life (at elevated ambient temperature) (see 3.20). Capacitors shall be tested in accordance with method 108 of MIL-STD-202. The following details and exceptions shall apply:

a. Mounting: Capacitors shall be mounted in accordance with 4.3.5.

b. Distance of temperature measurements from specimens: Not applicable.

c. Test temperature and tolerance: +125°C, +4°C, -0°C.

d. Procedure: Capacitors shall be subjected to the voltage and circuit specified in 4.6.3.2.1. In the event of a fuse failure, the procedure specified in 4.6.3.2.1 shall apply.

e. Test duration:

(1) Qualification:

(a) T level: 4,000 hours.

(b) M level: 1,000 hours.

(2) Group B: 1,000 hours.

f. Measurements during and after exposure: At the conclusion of 250, 1,000, 2,000, and 4,000 hours for T level, 1,000 hours for M level, and while the capacitors are at the applicable high-test temperature, the insulation resistance shall be measured in accordance with 4.6.4. At the option of the manufacturer, M level readings may also be taken at 250 hours. At the option of the manufacturer, the units may be immediately transferred (period of transfer not to exceed 15 minutes) to another chamber maintained at the same temperature for the purpose of measuring insulation resistance. The insulation resistance measurement shall be made only after the units have stabilized at the test temperature. The capacitors shall then be returned to the inspection conditions specified in 4.3 and shall be visually examined for evidence of mechanical damage and obliteration of marking (see 4.3.6); capacitance, dissipation factor, and insulation resistance shall be measured in accordance with 4.6.6, 4.6.7, and 4.6.4, respectively.

4.6.17 Dielectric voltage breakdown (see 3.21). Each capacitor in the sample shall be connected in series with an instrument to measure current. The current measuring instrument shall be capable of measuring in µA or mA. A dc voltage shall be gradually applied at no greater than 175 volts per second until failure occurs. Voltage at time of failure shall be recorded. If surface arcing occurs, the samples may be coated or immersed in a dielectric fluid such as peanut oil or a stable fluorocarbon-based insulating liquid.

NOTE: Care should be taken when testing high capacitance values (i.e. ≥ 4.7 µF). Initial in-rush or charging currents may exceed the equipment's "trigger" level; registering a failure prior to the capacitor experiencing breakdown.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be in accordance with the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The capacitors covered by this specification are intended for use in standard and high reliability military applications. High reliability applications include use in space and launch vehicles. Capacitors covered by this specification are unique due to the fact that they must be able to operate satisfactorily in standard and high reliability military systems under demanding conditions. These capacitors also offer reliability that is verified under a qualification system. Commercial components are not designed to withstand these military environmental conditions.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of this specification, the applicable specification sheet, and the complete PIN (see 1.2.1).

b. Packaging requirements (see 5.1 and 6.5).

c. Capacitor marking (see 3.22.3).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products that are, at the time of award of contract, qualified for inclusion in Qualified Products List whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from the DLA Land and Maritime, ATTN: VAT, PO Box 3990, Columbus, OH 43218-3990, or by email to vqp.chief@dla.mil.

6.3.1 Copies of SD-6, "Provisions Governing Qualification", are available online at http://quicksearch.dla.mil/.

6.4 Definitions.

6.4.1 Crack. A crack is a very slight separation along or across a boundary that usually occurs after sintering.

6.4.2 Delamination. A delamination is a significant separation along a material boundary or layer that occurs prior to or during sintering.

6.4.3 Chip-in. A chip-in is an area where ceramic can be seen to be forming a chip-out; however, the ceramic is still intact.

6.4.4 Chip-out. A chip-out is an area where ceramic has broken free from the capacitor.

6.4.5 Pinholes. A pinhole is a circular hollow or cavity.

6.4.6 Striations. Striations are vitrified layers without any actual separation.

6.5 Packaging guidance. When not specified in the contract or order (see 6.2), quantities of 250 capacitors or greater should be shipped on tape and reel and quantities less than 250 should be shipped in waffle packs. Bulk packaging is not recommended.

6.6 Soldering guidance.

6.6.1 Wave soldering. Wave soldering is not recommended for multiple layer ceramic capacitors (MLCC) larger than size 1206. Wave soldering uses liquid metal that has the highest heat transfer rate and is the hardest soldering method to use without shocking surface mount components. Extreme thermal shock is evidenced by visible cracks on the surface and sides of the capacitor. These cracks start at or near the termination and ceramic interface extending from the termination down along the capacitor edge. These surface cracks can become elliptical or circular shaped in the larger capacitor sizes. The cracks can eventually lead to failure of the capacitors. The manufacturer should be contacted for further information.

6.6.2 Manual soldering. Manual soldering with a soldering iron is not recommended for MLCCs. Damage due to thermal shock is common in MLCCs that are manually attached or reworked with a soldering iron. When manual soldering is absolutely necessary, hot air reflow is recommended. The manufacturer should be contacted for further information.

6.7 Tin whisker growth. The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions, on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to ASTMB545 (Standard Specification for Electrodeposited Coatings of Tin).

6.8 Subject term (key word) listing.

Base metal electrode
Precious metal electrode
Space
Ultrasonic inspection

6.9 Vicinal Illumination. For information regarding vicinal illumination, see S. Hull, “Nondestructive Detection of Cracks in Ceramics Using Vicinal Illumination”, ASM International, Nov. 1999, ISBN 0-87170-646-6.

6.10 Environmentally preferable material. Environmentally preferable materials should be used to the maximum extent possible to meet the requirements of this specification. As of the dating of this document, the U.S. Environmental Protection Agency (EPA) is focusing efforts on reducing 31 priority chemicals. The list of chemicals and additional information is available on their website http://www.epa.gov/osw/hazard/wastemin/priority.htm. Included in the EPA list of 31 priority chemicals are cadmium, lead, and mercury. Use of the materials on the list should be minimized or eliminated unless needed to meet the requirements specified herein (see section 3).

6.11 Changes from previous issue. Not applicable.

APPENDIX A

PROCEDURE FOR QUALIFICATION INSPECTION

A.1 SCOPE

A.1.1 Scope. This appendix details the procedure for submission of samples for qualification inspection of capacitors covered by this specification. The procedure for extending qualification of the required sample to other capacitors covered by this specification is also outlined herein. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 SUBMISSION

A.3.1 Sample. A sample consisting of 254 sample units, minimum, of the highest capacitance value in each voltage rating, in each voltage-temperature limits/temperature characteristic, in each termination, in each electrode material, in each group (see table A-I) for which qualification is sought shall be submitted. After qualification has been granted, no changes shall be made in materials, design, or construction without prior notification of the qualifying activity.

TABLE A-I. Qualification groups.

Group	Chip sizes
1	Smaller than 0805 (/1, /2, and /3)
2	0805 and larger (/4, /5, /6, /7, and /8)
3	0306 (/9) and 0508 (/10)
4	IDCs (/11 , /12, and /13)

A.4 EXTENT OF QUALIFICATION

A.4.1 Extent of qualification.

A.4.1.1 Chip size. Chip size qualification will be restricted to chip sizes equal to and smaller than the case size submitted within the group from which the submission was selected (see table A-I).

A.4.1.2 Capacitance. Capacitance-range qualification will be restricted to values equal to and less than the capacitance value submitted.

A.4.1.3 Voltage rating. Voltage rating qualification will be restricted to that submitted. Qualification may be extended to lower voltages than that submitted if the manufacturer can demonstrate that the capacitor design is the same.

A.4.1.4 Voltage-temperature limits / temperature characteristic. VTL/TC qualification will be restricted to that submitted. Qualification may be extended in accordance with table A-II if the manufacturer can demonstrate that the capacitor design uses the same dielectric material and the same or greater dielectric thickness per voltage rating.

TABLE A-II. VTL/TC extension of qualification.

Qualification of characteristic:	Will extend qualification to:
BP	C0G
BX	BR, BZ, BN, X7R, X7S
BR	BZ, BN, X7R, X7S
BZ	BN, X7R, X7S
BN	X7R, X7S
X7R	X7S

A.4.1.5 Termination. Termination qualification will be restricted to that submitted.

A.4.1.6 Electrode material. Electrode material qualification will be restricted to that submitted.

A.4.1.7 Product level. Qualification of any T level capacitor will extend qualification to the equivalent M level capacitor with the same design.

APPENDIX B

VISUAL INSPECTION CRITERIA FOR CHIP CAPACITORS

B.1 SCOPE

B.1.1 Scope. This appendix specifies the visual inspection criteria for chip capacitors. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

B.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

B.3 PROCEDURES FOR INSPECTION AND REJECTION

B.3.1 Method of inspection. Each capacitor shall be examined under 10 to 20 power magnification to determine compliance with the requirements specified herein.

B.3.2 Rejection criteria. Capacitors that deviate from the material, design, or construction requirements specified, or that fail to meet the following requirements, shall be unacceptable.

B.3.2.1 Termination metallization.

a. End terminals shall be completely covered. For chip sizes 0805 and larger, pinholes less than or equal to .005 inch (0.13 mm) in diameter are permitted (maximum of three pinholes in each surface area). For chip sizes smaller than 0805, pinholes less than or equal to .003 inch (0.08 mm) in diameter are permitted (maximum of three pinholes in each surface area).

b. Gaps in the metallization band shall only be acceptable if the metallization band is not less than the minimum metallization band requirement specified (see figure B-1).

c. Metallized edges shall not be reduced to less than 90 percent due to chipping or metallizing process (see figure B-2).

d. There shall be no excess metallization or solder tear which violates the minimum pad separation (see figure B-3).

e. There shall be no foreign material visibly adhering to the solder, or voids in the solder revealing greater than 10 percent of the base metallization (see figure B-4).

APPENDIX B

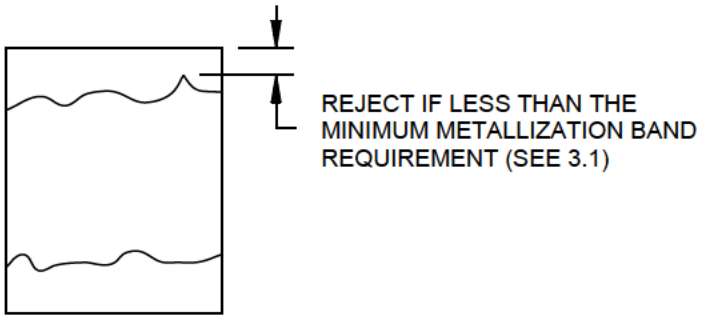


FIGURE B-1. Metallization band gaps.

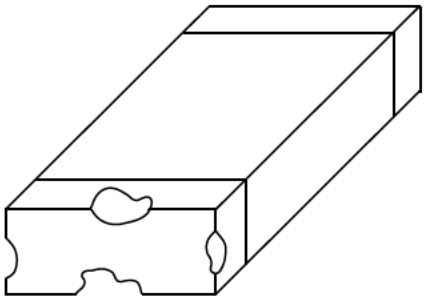


FIGURE B-2. Metallization band chipping.

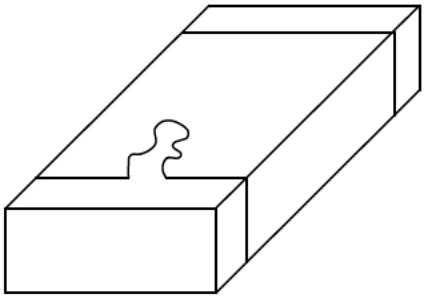


FIGURE B-3. Excessive metallization.

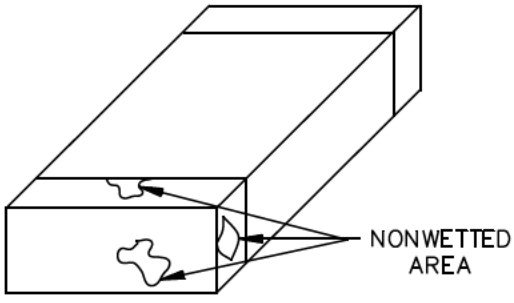


FIGURE B-4. Solder defects.

B.3.2.2 Ceramic surface examination.

a. There shall be no cracks (see 6.4.1) or chip-ins (see 6.4.3) (see figure B-5).

b. There shall be no delamination (see 6.4.2) of ceramic layers (see figure B-6).

c. Striations (see 6.4.6) are unacceptable (see figure B-6).

d. Chip-outs (see 6.4.4) shall not extend under the end termination or expose electrode plates (see figure B-7).

e. Rough edges shall be permitted provided they are within the allowable chip-out region as specified on figure B-7.

f. Lips, flared edges, or irregular shapes are unacceptable as specified on figure B-8.

g. There shall be no fused dust or excess material on external surface that prevents a chip from lying flat, or protrude more than .003 inch (0.08 mm) out of a surface.

h. There shall be no raised surfaces, bubbles, or blisters greater than .002 inch (0.05 mm) (usually found on top and bottom) (see figure B-9).

i. When compared to a flat surface, the clearance (warpage) at the center of the chip shall be less than 5 percent of the length dimension (see figure B-10).

j. There shall be no pinholes (see 6.4.5) larger than .002 inch (0.05 mm) in diameter (see figure B-11).

k. There shall be no holes (voids) that expose electrode plates (see figure B-12).

l. The marking shall be legible and complete (see figure B-13).

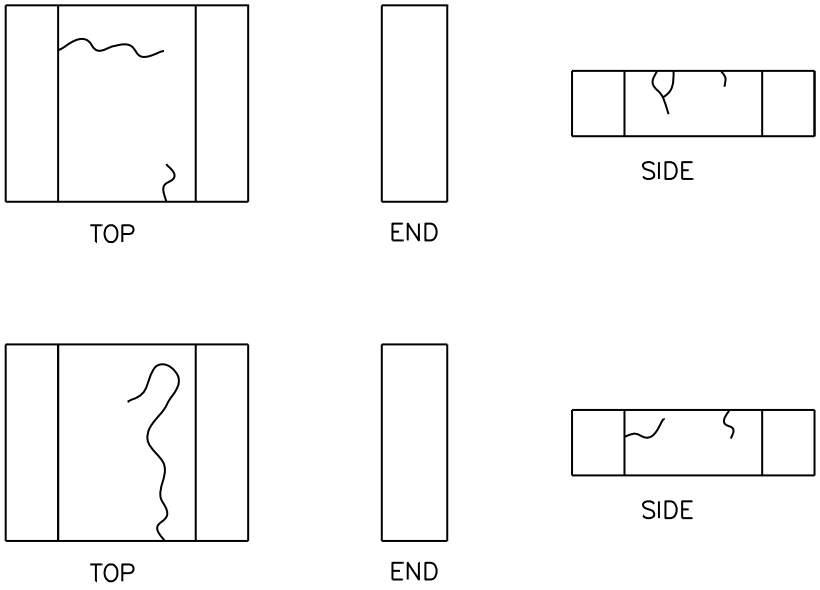


FIGURE B-5. Cracks.

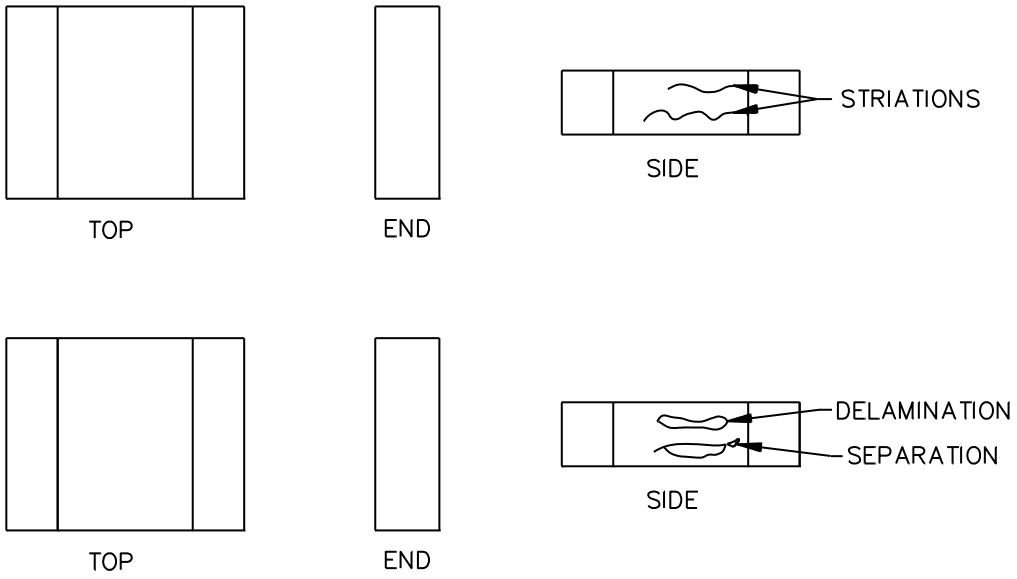


FIGURE B-6. Striations and delaminations.

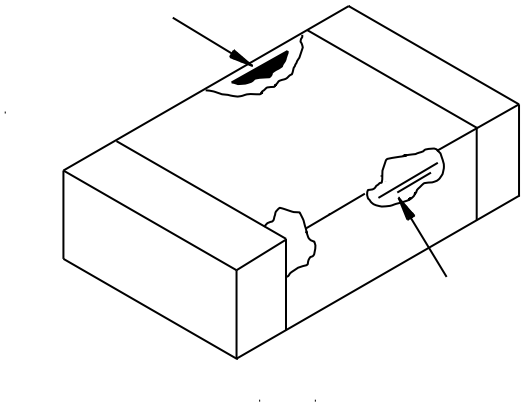


FIGURE B-7. Chip-outs.

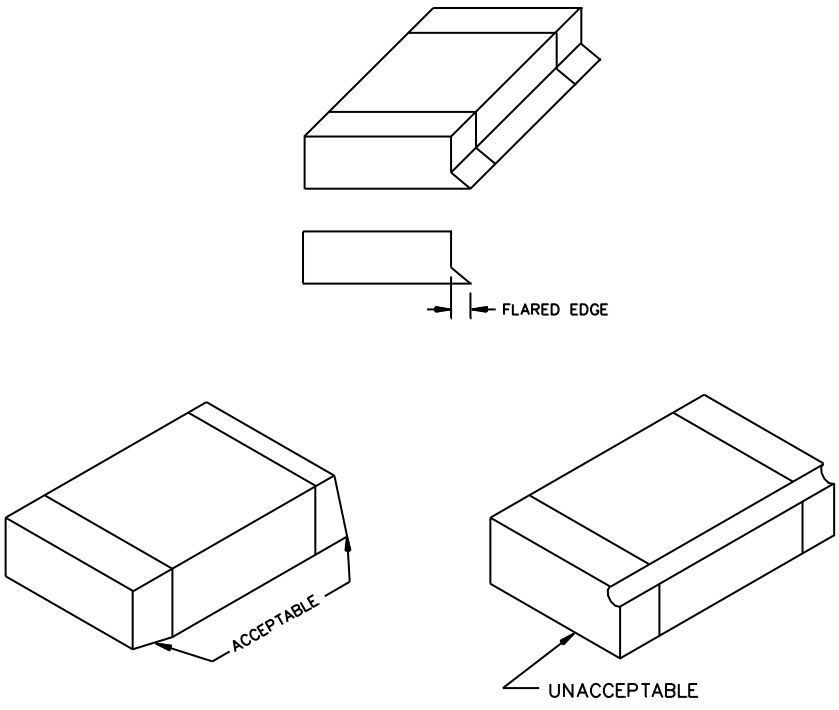


FIGURE B-8. Unacceptable lips, flared edges, or irregular shapes.

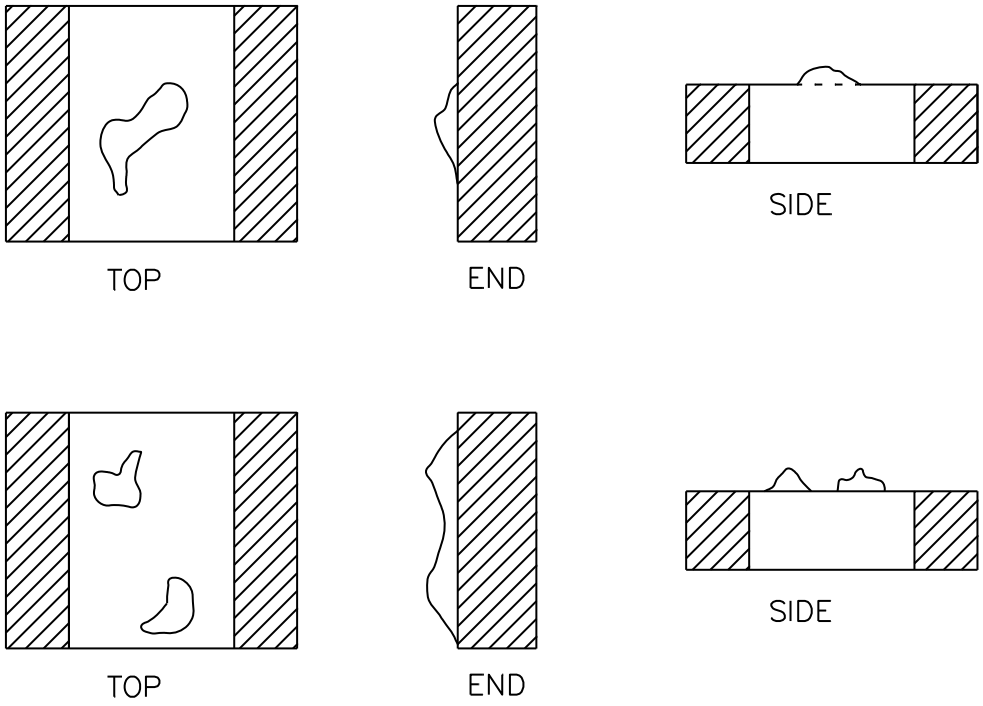


FIGURE B-9. Raised surfaces, bubbles, and blisters.

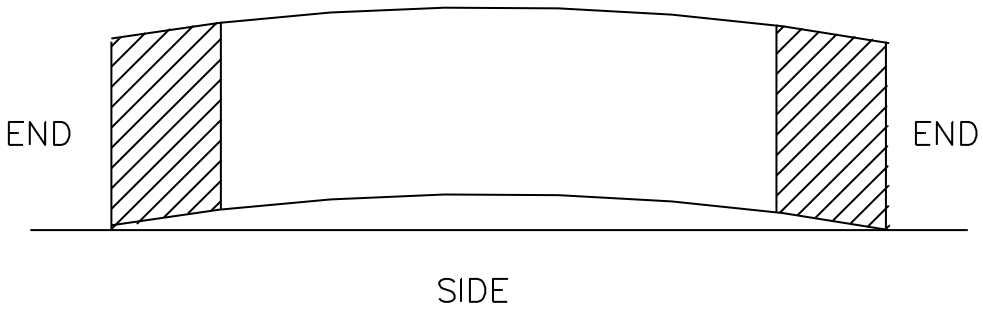


FIGURE B-10. Warpage.

FIGURE B-11. Pinholes.

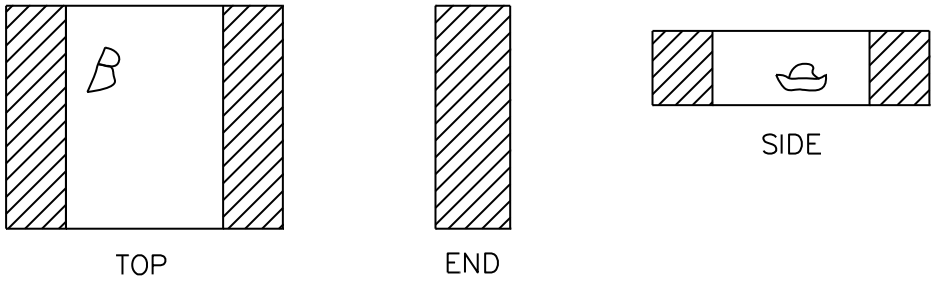


FIGURE B-12. Voids.

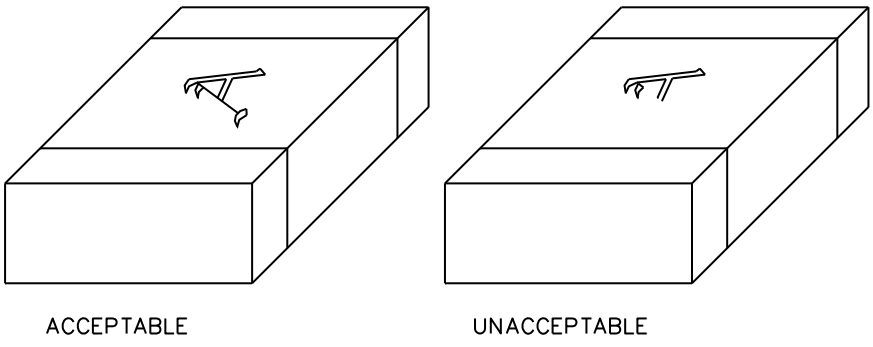


FIGURE B-13. Marking.

APPENDIX C

ULTRASONIC INSPECTION OF CERAMIC CAPACITORS

C.1 SCOPE

C.1.1 Scope. This appendix specifies the procedures and practices necessary for ultrasonic inspection of ceramic capacitors. Ultrasonic imaging is a nondestructive method for detecting internal physical defects in ceramic capacitors which are not otherwise visible. Ultrasonic imaging techniques are intended to reveal such flaws as delaminations, voids, and cracks. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

C.1.2 Definitions.

C.1.2.1 Bulk scanning. Bulk scanning is the process of using a single c-scan to image the entire thickness of the capacitor. Typically, the transducer is focused 50 percent into the capacitor.

C.1.2.2 C-scan. C-scan is a scan in an x-y plane with the z axis location fixed.

C.1.2.3 Double sided scanning. Double sided scanning is the process of using 2 c-scans to image a capacitor, where both scans have the capacitors oriented with the electrodes perpendicular to the sound wave. After the first scan, the capacitors are flipped over 180° and scanned a second time. Typically, the transducer is focused 25 percent into the capacitor.

C.1.2.4 False responses. When performing ultrasonic imaging, a response typically indicates the presence of air trapped in the capacitor body. The air is due to voids, delaminations, or cracks. When the response does not indicate the presence of air, it is a false response. False responses are typically seen when imaging non flat surfaces such as the edges of a capacitor or terminated surfaces.

C.1.2.5 Field of view: Field of view is the x-y area scanned. Optimal field of view is determined by multiplying the spot size by pixel density.

C.1.2.6 Reflection mode. Reflection mode uses one transducer to both send and receive ultrasound (often called pulse/echo).

C.1.2.7 Resolution. Resolution is the ability of a particular ultrasound system to discriminate closely spaced features. For a system using a focused transducer, the resolution is dependent on the material of the capacitor under test, the characteristics of the transducer, the characteristics of the pulser and receiver, the coupling fluid used, and software capability.

C.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

C.3 APPARATUS

C.3.1 Ultrasonic inspection equipment. The ultrasonic equipment shall be capable of performing c-scans in the reflection mode. The frequency will be such that the acoustic wave can penetrate the ceramic capacitor and image the back surface. If this is not possible, double sided scanning should be considered, but the depth that the sound wave will penetrate should be well understood. The resolution of the scan shall be adequate to detect defects as specified (see 4.6.1), relative to the size of the capacitor.

C.3.2 Output device. When specified (see 4.6.1), a hard or soft copy, grey (or color) scale image, shall be recorded for each capacitor scanned. The image or hard copy shall have sufficient resolution to meet the specified requirements (see 4.6.1). Maximum contrast shall be used to highlight rejects.

C.3.3 Holding tank. The holding tank shall be level and designed to hold the coupling fluid and locating fixtures without corroding or contaminating the capacitors under test.

C.3.4 Ultrasonic detector. Focused transducers capable of reflection mode imaging shall be used for inspection.

APPENDIX C

C.4 PROCEDURE

C.4.1 Mounting and handling. If offline inspection is used, capacitors shall be set-up in fixtures in order to identify and locate accept/reject pieces. Capacitors shall be fixtured so that the electrodes are perpendicular to the sound wave pulse from the transducer. If this is not possible, a second scan should be performed with the capacitors rotated 90° from the original scan. If any adhesive is used to fixture the capacitors, it shall be easily removed and not contaminate the capacitors. The coupling fluid is typically water or any other suitable fluid that will not contaminate the capacitors under test. Capacitors shall only be immersed in water for the time necessary to complete the imaging. Capacitors shall be cleaned and dried after imaging. Care shall be taken to ensure that no moisture remains trapped in the capacitors after drying.

C.4.2 Views. Unless otherwise specified (see 4.6.1), bulk scanning shall be used. Each capacitor shall be imaged at least once or as specified (see 4.6.1).

C.4.3 Recording and marking. Images used for accept/reject determination shall be of sufficient resolution to meet the specified requirements (see 4.6.1). Reject or unclassified capacitors shall be clearly noted on the records. Information stored with the records should clearly indicate the original identification of the image.

C.4.4 Identification. All capacitors must be identified prior to imaging. A detailed tally shall be kept of the number of capacitors inspected, number of capacitors accepted, and number of capacitors failed.

C.4.5 Set-up verification. Verification of the test set-up shall be carried out on periodic basis. Unless otherwise specified (see 4.6.1), the supplier shall determine the verification method to be used. The verification method used shall demonstrate that the set-up will find known defects and shall be approved by the qualifying activity.

C.4.6 Tests. The frequency of the transducer used shall be sufficient to resolve defects equal to or larger than the specified requirements (see 4.6.1), while still penetrating at least 50% (double-sided imaging) or 100% (single sided imaging) of the capacitor. Gate settings, receiver attenuation, and other equipment settings shall be selected to achieve the resolution specified (see 4.6.1).

C.4.7 Operating personnel. Personnel engaged in ultrasonic inspection shall have training in ultrasonic imaging procedures and techniques. They shall be certified by their employer to be capable of setting up and operating the equipment to meet the specified requirements (see 4.6.1) and ensuring that the accept/reject determinations are valid.

C.4.8 Interpretation of ultrasonic images. Ultrasonic images shall be inspected to determine that each capacitor meets the specified criteria (see 4.6.1). Hard copy or electronic images shall be of adequate resolution and lighting to make valid accept/reject determinations.

C.4.9 Examination and acceptance criteria. Capacitors shall be rejected when they have ultrasonic responses that indicate the presence of voids, cracks, or delaminations that exceed the allowances specified (4.6.1).

C.5 REPORT

C.5.1 Inspection record. The manufacturer or test facility shall maintain adequate verification of the results of the ultrasonic inspection. A complete record of the details of the inspection shall be kept by the manufacturer or test facility. If the capacitors are scanned at a location other than that of the manufacturer, the items listed below shall be included in the summary report provided to the manufacturer. The record or manufacturer's procedures shall include the following information:

a. Equipment used, including the transducer frequency, focal length, diameter, and serial number, if applicable.

b. Scan resolution.

c. Field of view / pixel density.

d. Fixturing method and adhesive used, if applicable.

e. Whether capacitors are terminated or unterminated.

f. Typical thickness of the capacitors imaged.

g. Number of capacitors scanned and the accept/reject quantities.

h. Date.

i. Name of operator.

j. Capacitor type or part number.

k. Capacitor manufacturer.

l. Ultrasonic laboratory, if other than capacitor manufacturer.

m. Typical scanned images for accept capacitors.

C.5.2 Summary of results. A summary of the results of the ultrasonic inspection shall be included in the group A data that is submitted to the acquiring activity with the capacitors (see 4.5.2.2b). At a minimum, this summary shall include the number of capacitors tested, number of capacitors rejected, and the date inspected.

C.5.3 Retention. All ultrasonic images and reports shall be maintained for the period specified (see 4.2.3).

C.6 CALCULATIONS

C.6.1 Fundamental resolution of transducer (λ):

$$\lambda = {}^{c}/_{f}$$

Where: λ = wavelength
c = material sound velocity
f = frequency

NOTE: For detection, the flaw must be a minimum of half the wavelength.

C.6.2 F number ($F\#$):

$$F\# = {}^{Focal\ length}/_{Diameter}$$

C.6.3 Spot size (ΔX):

$$\Delta X = 1.22 \times F\#({}^{\lambda}/_{2})$$

C.6.4 Resolution of focused transducer in reflection mode (R):

$$R = .707\Delta X$$

C.6.5 Depth of field (ΔZ):

$$\Delta Z = 7.1(F\#)^{2}({}^{\lambda}/_{2})$$

C.6.6 Example.

For a 50 MHz transducer with a focal length of .5 inch, a diameter of .250 inch, and using $5.53x10^3$ m/s as the velocity of sound in barium titanate:

$$\lambda = {5.53x10^3}/{50x10^6} = .00011\,m = .0044\,inch$$

$${\lambda}/{2} = 55\,\mu m = .0022\,inch$$

$$F\# = {\cdot 5}/{.25} = 2$$

$$\Delta X = 1.22 \times 2(.0022) = .0054\,inch$$

$$R = .707(.0054) = .0038\,inch$$

$$\Delta Z = 7.1(2)^2(.0022) = .0625\,inch$$

TABLE C-I. Typical transducer resolution and depth of focus for barium titanate based ceramic capacitors.

Transducer frequency (MHz)	Fundamental resolution (µm)	(inches)	Focal length (inches)	Diameter (inches)	F#	Spot size (inches)	Theoretical resolution (inches)	Optimal FOV (@512, in)	Optimal FOV (@1024, in)	Depth of focus (inches)
10	275	.0100	2.000	.500	4	.0488	.03450	24.9856	49.9712	2.2720
10	275	.0100	.750	.375	2	.0183	.01294	9.3696	18.7392	.5680
15	180	.0070	.750	.500	1.5	.0128	.00906	6.5587	13.1174	.2237
20	137	.0050	1.250	.250	5	.0153	.01078	7.8080	15.6160	1.7750
20	137	.0050	.500	.250	2	.0061	.00431	3.1232	6.2464	.2840
30	92	.0036	1.250	.250	5	.0110	.00776	5.6218	11.2435	1.2780
30	92	.0036	.750	.250	3	.0066	.00466	3.3731	6.7461	.4601
30	92	.0036	.500	.250	2	.0044	.00311	2.2487	4.4974	.2045
50	55	.0022	1.000	.250	4	.0107	.00759	3.7478	7.4957	.2499
50	55	.0022	.500	.250	2	.0054	.00381	1.8739	3.7478	.0625
75	38	.0015	.500	.250	2	.0018	.00129	.9370	1.8739	.0852
100	25	.0010	.500	.250	2	.0012	.00086	.6246	1.2493	.0568
100	25	.0010	.200	.250	0.8	.0005	.00035	.2499	.4997	.0091

Custodians:
Army – CR
Navy - EC
Air Force – 85
DLA - CC

Preparing activity:
DLA - CC

(Project 5910-2013-026)

Review activities:
Army - MI
Navy - AS, MC, OS, SH
Air Force - 19, 99
Other – MDA, NA

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.