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MILITARY HANDBOOK

DOSE-RATE HARDNESS ASSURANCE GUIDELINES

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DISTIBUTION STATEMENT A.

Approved for public release; distribution is unlimited

FOREWORD

1. This military handbook is approved for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Space and Naval Warfare Systems Command, Washington DC 20363-5100, by using the self-addressed *Standardization Document Improvement* Proposal (DD Form 1426) appearing at the end of this document or by letter.

CAUTION

THIS DOCUMENT HAS BEEN ASSEMBLED AS A GUIDELINE FOR THE DEVELOPMENT OF A DOSE-RATE HARDNESS ASSURANCE PROGRAM FOR SEMICONDUCTOR ELECTRONICS. IT IS NOT INTENDED TO BE USED AS A REQUIREMENTS DOCUMENT. THIS DOCUMENT MAY NOT CONTAIN ALL THE INFORMATION NEEDED TO ESTABLISH SUCH A PROGRAM.

PREFACE

Preparation of this handbook has been carried out under the direction of Defense Nuclear Agency (DNA), and their contracting officers Major B. Hickman and LCDR L. Cohn. Many individuals in the hardness assurance community have contributed significantly to the preparation of this document by preparing text, offering comments, and reviewing draft documents. Special thanks must be given to Mr J. Ferry (AFWL) who has served as the project monitor for this work; Dr. Eligius Wolicki who served as the DNA Program Area Reviewer for Hardness Assurance and the Chairman of the Space Parts Working Group Hardness Assurance Committee; and to Dr. Harvey Eisen, the present DNA Program Area Reviewer for Hardness Assurance. Special acknowledgement is given to William Alfonte (KAMAN-TEMPO), Tom Ellis (NWSC), Joseph Halpin (HDL), John Harrity (IRT), Arthur Namenson (NRL), Ron Pease (MRC) Robert Poll (JAYCOR) who have contributed significantly to the preparation of this document. Without the aid and expert knowledge of all of these individuals and the Hardness Assurance Committee of the NASA/SD Space Parts Group, the development of this document would not have been possible.

CONTENTS

1. SCOPE

1.1 Scope. The scope of this document is limited to dose-rate radiation effects on semiconductor electronics and is specifically intended to address hardness assurance at the piece-part level. Because the nature of dose-rate effects sometimes requires a close interaction between system hardness assurance and piece-part hardness assurance, some system requirements are also discussed.

1.2 Users of this document. This document is written primarily for those individuals who are involved with hardness assurance activities. It also provides a guide for designers of radiation hardened systems and, as a result, is an aid in developing hardness assurance design documentation (HADD).

1.3 Document application. This document primarily discusses piece-part hardness assurance methods for the dose-rate environment, and addresses system hardness assurance topics only as they are necessary to complete the discussion of piece part hardness assurance. Thus, the discussion will deal with the radiation categorizing of piece-parts according to certain criteria, which will determine the controls needed during part procurement. Specific activities and functions which may be significantly different for different systems and for different contracting organizations will not be discussed in detail in this document.

1.3.1 Dose-rate dependent problems. Certain dose-rate dependent problems, such as burnout and latchup, cannot effectively be handled at the piece-part level. In these cases, system- and circuit-level, or both design solutions may be the most effective means of ensuring survival.

1.4 Effects. This section provides a brief overview of the important elements of dose-rate hardness assurance. The following sections of the document will address some of these issues in greater detail. A summary of dose-rate effects is shown on figure 1.

1.4.1 Photocurrents. The dose-rate environment produces transient current surges in semiconductor devices. In a single junction, the current is called photocurrent (I_p) and flows in the direction of junction leakage current. In transistors, the current surge in the collector-base junction is called the primary photocurrent (I_{pp}) and may, in certain cases, be amplified by the transistor gain to produce secondary photocurrents (I_{sp}).

1.4.2 Discrete devices. In discrete devices, the photocurrent may appear as a transient noise pulse, interfering with the normal operation of the device or the circuit in which it is used. If the radiation is intense enough and if the resulting energy deposited in the device is great enough, the device may burn out.

1.4.3 Integrated circuits. Dose-rate effects in integrated circuits are similar to the effects observed in discrete devices. One common term which is used to describe the dose-rate effect in integrated circuits is "upset." The device is said to have upset when the dose-rate effect results in the device being in an unwanted operating state as a result of the radiation. For example, the dose rate response of bipolar linear circuits may appear as an output voltage transient lasting 10 or more microseconds, along with power supply surge currents. Digital circuits may experience a change in output state, a change of state of stored data (bit flip), or simply a deviation in output voltage which is defined as being unacceptable for proper operation of the device. In most cases, the device will recover and continue to function normally, once the radiation pulse terminates and the induced transient subsides. However, if sufficient energy is available, the device may be damaged and may not recover after the radiation pulse.

1.4.4 Latchup. In both linear and digital integrated circuits, the device may experience an effect called four-layer latchup. Should the device enter a latchup condition, the circuit will cease to operate normally, and may in fact burn out. A summary of these effects is shown on figure 1.

1.5 Part categories by effect. It should be noted that the parts must be categorized separately for each dose-rate radiation effect. For example, a dielectrically isolated integrated circuit may be judged to be HNC for latchup but a HCC-1 for upset. Therefore, the device would be categorized as HCC-1.

1.6 Documentation. Hardness assurance for piece parts takes place during the system production and parts procurement phases. The tests and screens which were determined during the design phase, and are described in detail in the hardness assurance design documentation (HADD), are put into effect during the hardness assurance phase.

1.6.1 Design documentation. This is a collection of information on the design hardening techniques used, the survivability/vulnerability analysis, configuration and quality control, test data, procurement specifications, management, and any other information necessary for production of the system: 1/

1.6.1.1 Typical documentation. These documents may vary between systems, but a common set would contain the following:

a. An introduction. Providing a general systems operation and functional description.

b. An HCI Index. Providing a hardness critical item list which relates hardness critical parts to their application. The hardness criticality is indicated and cross-referenced to analysis.

c. A hardness assurance plan. Presenting the management organization and technical requirements which are to be implemented throughout the production period.

d. An analysis discussion. Containing the survivability/vulnerability analysis and any related information.

1/ For a more complete description of the HADD, see 6.1 herein.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATIONS

MILITARY

MIL-S-19500 - Semiconductor Devices, General Specifications for.

MIL-M-38510 - Microcircuits, General Specifications for.

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-202 - Test Methods for Electronic and Electrical Component Parts.

MIL-STD-750 - Test Methods for Semiconductor Devices.

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

MIL-STD-45662 - Calibration Systems Requirements.

HANDBOOKS 2/

MILITARY

MIL-HDBK-279 - Total Dose Hardness Assurance Guidelines for Semiconductor Devices and Microcircuits.

MIL-HDBK-280 - Neutron Hardness Assurance Guidelines for Semiconductor Devices and Microcircuits.

MIL-HDBK-816 - Guidelines for Developing Radiation Hardness Assurance Device Specifications.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.1.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those cited in the solicitation.

DODISS - Department of Defense Index of Specifications and Standards.
DNA 5910F - Piece-Part Neutron Hardness Assurance Guidelines for Semiconductor Parts.
DNA 5909F - Total Dose Hardness Assurance Guidelines.
DNA 5928 - Latchup Analysis of Bipolar Integrated Circuits.
DNA 5913 - Upset Response Testing of MSI Integrated Circuits.

2/ MIL-HDBK-815 will supersede MIL-HDBK-279 and MIL-HDBK-280 when available.

(Copies of Defense Nuclear Agency (DNA) guidelines and reports are available from the Defense Nuclear Agency, 6801 Telegraph Road, Alexandria, VA 22310-3398. Copies of the DODISS are available on a yearly subscription basis either from the Government Printing Office for hard copy, or microfiche are available from the Director, Navy Publications and Printing Service Office, 700 Robbins Avenue, Philadelphia, PA 19111-5093.)

2.2 Non-Government publications. The following documents form part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM E665 - Standard Practice for Determining Absorbed Dose Versus Depth in Materials Exposed to the X-Ray Output of Flash X-Ray Machines.

ASTM E666 - Standard Practice for Calculating Absorbed Dose from Gamma or X Radiation.

ASTM E668 - Standard Practice for the Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.

ASTM E820 - Standard Practice for Determining Absolute Absorbed Dose Rates for Electron Beams.

ASTM F448 - Standard Test Method for Measuring Steady-State Primary Photocurrent.

ASTM F526 - Standard Test Method for Measuring Dose for Use in Linear Accelerator Pulsed Radiation Effects Tests.

ASTM F675 - Standard Test Method for Measuring Nonequilibrium Transient Photocurrents in p-n Junctions.

ASTM F744 - Standard Test Method for Measuring Dose Rate Threshold for Upset of Digital Integrated Circuits.

ASTM F773 - Standard Practice for Measuring Dose Rate Response of Linear Integrated Circuits.

(Application for copies should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103-1187.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Acronyms used in this handbook. The acronyms used in this handbook are as follows:

a. CCB - Configuration Control Board

b. HA - Hardness assurance

c. HADD - Hardness assurance design documentation

d. HCC - Hardness critical category

e. HCI - Hardness critical item

f. HM - Hardness maintenance

g. HNC - Hardness noncritical

h. PMPCB - Parts, material and process control board

i. SPO - System Project Office. The SPO is the overall controlling organization for the project under consideration. It is intended to be a generic term so as to standardize, for the purposes of this document, such expressions as system, system project, Project Manager's Office, Project Manager, procurement agency, and contracting agency.

3.2 Definitions and symbols. For the purpose of this handbook the following definitions and symbols shall apply.

3.2.1 Burnout. Burnout is the failure of a device subjected to electrical overstress. Typically, thermal damage has occurred within one or more device junctions or within the device metallization.

3.2.2 Confidence level. Confidence level (C) is the probability (usually given in percent) that at least a portion, (P_{DIST}) of the parts in the lot will survive.

3.2.3 Cumulative probability. Cumulative probability (P_{DIST}) is the percentage or proportion of a probability distribution which is below a given upper limit for above a given lower limit.

3.2.4 Design margin break point. Design margin break point (DMBP) is a categorization method which provides a criterion which may apply to all parts in a system and is based on a single fixed value of design margin.

3.2.5 Dose rate. Dose rate ($\dot{\gamma}$) is the dose rate level under consideration. It is usually stated in interims of rads(Si)/second.

3.2.6 Dose rate design margin. Dose rate design margin ($DM_{\dot{\gamma}}$) is the ratio of the mean failure dose rate to a specified dose rate.

3.2.7 Dose rate to failure value. Dose rate to failure value ($\dot{\gamma}_{FAIL}$) is the dose rate level for the part under test at which a parameter designated as PAR_{RAD} equals PAR_{FAIL}.

3.2.8 Environment. Dose rate effects may be caused by a variety of ionizing radiation environments. These environments may consist of neutrons, photons, electrons, or single particle ionization. The methods which are used to harden against the various environments may vary from one environment to another. For example, shielding can be an effective tool for some low energy x-rays but may be ineffective for higher energy gamma rays. In contrast, even though the hardening methods may be different, one may find that the hardness assurance procurement procedures may be similar regardless of the environment.

3.2.9 Hardness assessment. Hardness assessment is the determination of the susceptibility to damage or upset of a system, subsystem or component.

3.2.10 Piece-part hardness assurance. Piece-part hardness assurance is the application of production controls and tests to the procurement of an electronic part to ensure that its radiation response is within acceptable limits.

3.2.11 System hardness assurance. System hardness assurance consists of the procedures applied during system fabrication, and procurement to ensure that the system maintains a nuclear response that stays within acceptable limits.

3.2.12 Hardness maintenance. Hardness maintenance is the combination of inspection, test, and repair activities accomplished on a hardened system to ensure that the hardness designed into the system is retained throughout the system lifetime.

3.2.13 Hardness surveillance. Hardness surveillance consists of the long term inspection and test procedures, performed beyond hardness maintenance, which are conducted to assure that systems are properly maintained with the desired hardness.

3.2.14 Hardness verification. Hardness verification is the determination through a careful sequence of tests and analyses that a system design is in fact hardened in compliance with the nuclear specification.

3.2.15 Latchup. Latchup in integrated circuits is an abnormal operating state usually characterized by the failure of a device to respond properly to input conditions, and the presence of abnormally high currents or both flowing in the device. Latchup is usually caused by the regenerative action of four layer (PNPN) conduction paths within the device.

3.2.16 Lot. Lot is the collection of parts from which the sample has been taken (see MIL-M-38510).

3.2.17 Lot acceptance. Lot acceptance test is the test of a sample of parts from a procurement lot to determine if the lot is acceptable. For the purpose of hardness assurance, this term is intended to be a generic term in order to standardize on commonly used expressions such as lot conformance test, quality conformance test, or quality conformance inspection.

3.2.18 Lot size. Lot size (N) is the number of parts in the lot before the sample has been removed.

3.2.19 Mean dose rate to failure. The mean dose rate failure for $(\dot{Y}_{MF})$.

$$\dot{Y}_{MF} = \exp\left[\overline{\ell n(\dot{Y}_{FAIL})}\right] \dot{Y}$$

3.2.20 Measured logarithmic mean. Measured logarithmic mean for PAR_{RAD} $[\ell n(PAR_{RAD})]$.

$$\overline{\ell n(PAR_{RAD})} \equiv \frac{1}{n} \sum_{i=1}^{n} \ell n(PAR_{RAD_i})$$

3.2.21 Measured logarithmic mean. Measured logarithmic mean for $\dot{Y}_{FAIL}$ $[\overline{\ell n(\dot{Y}_{FAIL})}]$.

$$\overline{\ell n(\dot{\gamma}_{FAIL})} \equiv \frac{1}{n}\sum_{i=1}^{n} \ell n\,(\dot{\gamma}_{FAIL_i})$$

3.2.22 Measured logarithmic standard deviation. The measured logarithmic standard deviation for $\dot{\gamma}_{FAIL}$ $[s_{\ell n}(\dot{\gamma}_{FAIL})]$.

$$s_{\ell n}(\dot{\gamma}_{FAIL}) \equiv \left(\frac{1}{n-1}\sum_{i=1}^{n} [\ell n(\dot{\gamma}_{FAIL_i}) - \overline{\ell n(\dot{\gamma}_{FAIL})}]^2\right)^{1/2}$$

3.2.23 Measured logarithmic standard deviation. Measured logarithmic standard deviation for PAR_{RAD} $150[s_{\ell n}(PAR_{RAD})]$.

$$s_{\ell n}(PAR_{RAD}) \equiv \left\{ \frac{1}{n-1}\sum_{i=1}^{n} [\ell n(PAR_{RAD_i}) - \overline{\ell n(PAR_{RAD})}]^2 \right\}^{1/2}$$

3.2.24 Measured mean. Measured mean for $PAR(\overline{PAR})$.

$$\overline{PAR} \equiv \frac{1}{n}\sum_{i=1}^{n} PAR_i$$

where PAR_i is the parameter value measured for the i^{th} device.

3.2.25 Measured standard deviation. Measured standard deviation for PAR_{RAD} $[s(PAR_{RAD})]$,

$$s(PAR_{RAD}) \equiv \left\{ \frac{1}{n-1}\sum_{i=1}^{n} (PAR_{RAD_i} - PAR)^2 \right\}^{1/2}$$

3.2.26 One-sided tolerance limit. One-sided tolerance limit (Kn) is the number of standard deviations from the mean which defines a limit on a normally distributed parameter (PAR), with confidence C that the parameter in the parent population is greater than

$$PAR - K_{TL}(n, C, P_{FAIL}) \times S(PAR)$$

or less than

$$PAR - K_{TL}(n, C, P_{FAIL}) \times S(PAR).$$

3.2.27 Parameter failure value. Parameter failure value (PAR_{FAIL}) is the value of a particular parameter for the device under evaluation at which circuit failure is defined to occur. This value is application *dependent*.

3.2.28 Parameter specification value. Parameter specification value (PAR_{MIN} or PAR_{MAX}) is the specified minimum or maximum device parameter value prior to irradiation. This value is usually given by the manufacturer.

3.2.29 Parameter design margin. Parameter design margin (DM)

$$DM = PAR_{FAIL} \; / \; \exp\left[\overline{\ell n PAR_{RAD}}\right]$$

for parameters which increase with radiation, and

$$DM = \exp\left[\overline{\ell n (PAR_{RAD})}\right] \; / \; PAR_{FAIL}$$

for parameters which decrease with radiation, where PAR_{RAD} is evaluated at $\dot{Y}_{SPEC}$.

3.2.30 Part. Part (piece part) is the electronic device used in a specific circuit application or test.

3.2.31 Part categorization criterion. Part categorization criterion (PCC) is a categorization method which sets a separate criterion to categorize each particular part type used in a system. The DM of each part type is compared to its PCC to determine its part category.

3.2.32 Part parameter value. Part parameter value (PAV) is the electrical parameter value measured for a device.

3.2.33 Radiation-induced parameter value. Radiation-induced parameter value (PARRAD) is the value of a parameter at a particular radiation level.

3.2.34 Sample size. Sample size (n) is the number of parts, selected at random from the lot, to be tested.

3.2.35 Specified dose rate. Specified dose rate ($\dot{Y}_{SPEC}$) is the maximum dose rate which the circuit under consideration must withstand.

3.2.36 Survivability level. Survivability level is the radiation level which the device, circuit or system can withstand without suffering an impairment of its ability to accomplish its function.

3.2.37 Symbols.

C	Confidence level
DM(PAR)	Parameter design margin
DMBP	Design margin break point
DM	Dose rate design margin
$\dot{Y}_{FAIL}$	Dose-rate-to-failure value
$\dot{Y}_{MF}$	Mean dose rate to failure
$\dot{Y}_{SPEC}$	Specified dose rate

$\dot{Y}_{CIRC}$	Circumvention dose rate
I_p	Junction photocurrent
I_{pp}	Primary photocurrent
I_s	Circuit saturation current
I_{sp}	Secondary photocurrent
I_T	Terminal current
I_{TH}	Threshold current
K_{TL}	One-sided tolerance limit factor
$\ell n(PAR_{RAD})$	Measured logarithmic mean for PAR_{RAD}
$\ell n(\dot{Y}_{FAIL})$	Measured logarithmic mean for $\dot{Y}_{FAIL}$
n	Sample size
N	Lot size
PAR	Device parameter value
PAR_{FAIL}	Parameter failure value
PAR_{MIN} or PAR_{MAX}	Specified parameter value (minimum or maximum)
PAR_{RAD}	Radiation-induced parameter value
PCC	Part categorization criterion
$s_{\ell n(PAR_{RAD})}$	Standard deviation for PAR_{RAD}
$s_{\ell n(\dot{Y}_{FAIL})}$	Measured logarithmic standard deviation for $\dot{Y}_{FAIL}$
P_{DIST}	Cumulative proportion of distribution
t_{rec}	Recovery time
t_{spec}	Allowable recovery time

3.2.39 Vulnerability level. Vulnerability level is the level at which the device is considered to have failed the functional requirement.

4. DESIGN HARDENING

4.1 *Overview of dose-rate design hardening*. Dose rate design hardening is the iterative process by which the system requirements are assessed, the circuits are designed, parts are selected, and circuit susceptibility is assessed to achieve an optimally hardened circuit design. The system specifications are met by hardening methods such as part selection, current-limiting, photocurrent compensation, power management, shielding, and other methods. The following sections describe those specific aspects of design hardening which affect dose-rate hardness assurance and outline the general requirements for radiation design hardening. The output of the design hardening program as required for hardness assurance is discussed.

4.1.1 Radiation design hardening. Radiation design hardening consists of circuit design, parts selection, and hardness assessment activities performed to achieve an optimum and cost-effective circuit design that will be survivable in a given radiation environment.

4.1.2 Dose-rate hardening methods. Dose-rate hardening methods cannot usually be limited to a single technique which applies to all effects. In addition, many of the techniques used involve circuit or system-level consideration and do not necessarily depend on specific device characteristics. In general, hardening techniques fall into three categories:

a. Those which deal with the devices and, therefore, are strongly influenced by the choice of devices (e.g., dielectric isolation).

b. Those which use a circuit or system solution that depends on knowledge of the device characteristics, (e.g., current limiting).

c. Those which use a circuit or system solution that does not directly depend on the specific device characteristics, (e.g., circumvention).

4.1.3 Design hardening process. Once system analysis has determined that dose-rate hardening is required, the process of design hardening begins and produces several results that are required for the hardness assurance program. The following steps are required to carry out a successful program;

a. Determination of hardening measures.

b. Determination of the circuit failure criterion for each part application and dose-rate effect on the basis of worst-case analysis.

c. Determination of the mean-dose-rate-to-failure which causes the circuit or device to fail.

d. Identification of the characterization data, data source, and quality of data used for the determination of failure.

e. Determination of the device design margins.

f. Determination of the part categorization criteria, PCC, or the DMBP value. The device design margins are compared to the categorization criteria to determine test and control criteria.

g. Categorization of the part for each application and effect being evaluated.

4.1.4 Statistical qualification. In some cases, where little data are available, part characterization may be used to qualify devices on a statistical basis. Statistical qualification requires that the population of devices has a statistically well behaved dose-rate response which follows a known distribution. In other situations where the part response is extremely variable, a worst-case estimate of the bound of the statistical distribution may be used.

4.1.5 Small design margins. Part types with very small design margins should be eliminated from use in the system. The decision as to when a design margin is small enough to make the part unacceptable will depend on the cost of rejecting lots during hardness assurance versus the cost of either using a less sensitive part type or redesigning the circuit. Since these costs are highly dependent on the specific part type and the specific system in which the part is used, no one formula for determining a minimum acceptable design margin can apply to all situations. Two suggested general rules for selecting parts are:

a. Part types with design margins 1 or less will not be used.

b. Part types with design margins between 1 and 2 are generally unacceptable, and should be used only if no alternatives are available. On the basis of calculations for silicon bipolar transistors, a relatively high rate of lot rejection and part failure or both is to be expected when parts with design margins less than two are used. The actual rejection rate and risk will depend on the part distribution and the variance of that distribution.

4.1.6 Part selection. During design hardening, one of the most effective steps for reducing hardness assurance costs is the proper selection of radiation-resistant parts. This is particularly important for dose-rate effects, since some of these effects are most efficiently handled by the choice of proper parts.

4.1.6.1 Device design fabrication parameters. Device design fabrication parameters may be an important factor in controlling the dose-rate response of a device (see figure 1). For example, parts with dielectric isolation, gold doping, buried layers or other techniques, may be used to avoid latchup. Internal photocurrent compensation may be used to improve the threshold for upset. These kinds of factors need to be considered when components are being selected. Parts with smaller geometry, having lower photoresponse, might be substituted for parts with unacceptably large photoresponse. Parts with higher thresholds for upset or burnout may be substituted for others.

4.1.7 Circuit design features. The use of special circuit design features may be an effective system solution to accomplish hardening for the dose rate environment. The use of low voltages and long circuit time constants may be an effective hardening method. Low voltages reduce the probability of latchup, while long circuit time constants may raise the upset threshold of the device.

4.1.7.1 Current limiting. Current limiting is a hardening technique which, through circuit design, limits the maximum current which may be delivered to the device. In general, current limiting can be an effective means of increasing the immunity of the device to burnout and preventing latchup.

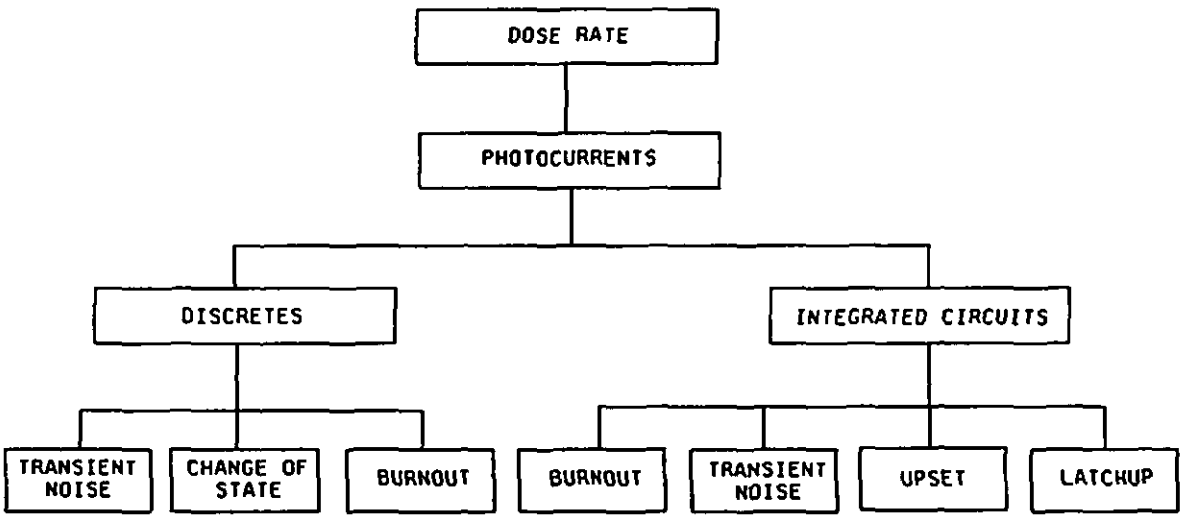

FIGURE 1. Response tree for dose-rate effects.

4.1.8 System level solutions. Like part selection, circuit design hardening can be a very effective way of reducing the hardness assurance effort. Again, if a circuit can be redesigned to change the classification of a part from radiation sensitive to insensitive, such redesign may be highly cost-effective over the life cycle of the system. Although the subject is very complex and a complete treatment is beyond the scope of this document, the following suggestions are considered:

a. Where possible, circuits should be designed so as to maximize the use of intrinsically-hard parts, and to minimize the use of costly radiation hardened parts.

b. Circuits should be designed to minimize sensitivity to the transient dose-rate response.

c. Limiting resistors should be used to protect devices from burnout and to reduce latchup sensitivity.

d. System or circuit design solutions should be considered for devices where a design margin approach is not possible. For example, devices that are susceptible to latchup do not usually lend themselves to a design margin approach. In this case a power management technique, where power is momentarily removed, would be a possible alternative at the system level.

4.1.8.1 Circumvention and power management. It is not always feasible to eliminate all devices which are latchup-prone from the system design. Therefore, the possibility of device latchup must be eliminated by other means. Often, some form of power management is used in circuit design. Either the power is periodically removed from the device through a method of power strobing, where the device power is periodically removed, or power is removed upon the detection of radiation, as in circumvention.

4.1.8.2 Fault-tolerant design. The area of fault-tolerant design is beyond the scope of this document. For the present, it is sufficient to note that some circuits are able to tolerate the upset or failure of some devices. In upset-tolerant circuits, the devices are usually linear or combinatorial logic devices and are restored to their correct operating conditions after the radiation pulse. Man-attended equipment may even be allowed to tolerate latchup, blown fuses and tripped circuit breakers.

4.1.8.3 Shielding. For space systems, prompt dose-rate effects are the result of the sum of the x-ray and prompt gamma-ray induced transient ionization. The dose rate caused by the x-rays is usually dominant over the gamma-ray dose rate. The x-ray dose rate can be reduced with shielding. Let environment cannot practically be reduced with shielding for missile or airborne systems. Thus, shielding is in general only practical to reduce the x-ray component to the level of the $\dot{Y}$ component. For systems which must operate through an event, this can be important since the gamma rays alone can induce circuit upset. It should be noted that some shields used to reduce the x-ray dose can cause IEMP problems and techniques such as using low-Z coating material may be required to reduce electron emission on certain space or airborne systems. For some ground-based systems, large amounts of shielding may be possible. Concrete bunkers or other heavy shields may be considered.

4.1.8.3.1 Space system shielding. In many space systems, dose-rate effects can be greatly reduced through the use of some careful design factors and judicious shielding. Some simple design rules that are often used are:

a. Bury sensitive components deep in the system, for self-shielding.

b. Group sensitive components together for mutual protection and shadowing and more economical shielding.

c. Locate such groupings near massive structural elements.

d. Increase chassis and structural element thickness in selected areas for increased shielding.

e. Include small local device shields for additional dose rate reduction.

4.1.8.3.2 Weight penalty. It is important to note that the weight penalty for extensive and massive shielding is often prohibitive for space or airborne systems, and device location is often dictated by circuit requirements which may preclude locating the part in an optimum location for shielding. New packaging techniques are being developed, which incorporate shielding as part of specially constructed packages (see 6.1.4 herein).

4.2 Part categorization methods. As part of the design phase, it is necessary to determine the radiation response of the part types, and to classify the parts with regard to the need for hardness assurance. The categorization of the part types is performed in accordance with 5 herein.

4.2.1 Categorization of parts. Categorization of parts is more complex for dose-rate effects than for other radiation effects. Because of the multiplicity of effects in the dose-rate environment, each effect should be considered separately. For example, a part may be protected from burnout by providing adequate current-limiting but may still be sensitive to upset. Thus, the part would be examined for each failure mode identified in the design.

4.2.2 Failure modes. Fortunately, some failure modes such as upset are nondestructive and, therefore, may be handled using a 100 percent screen to ensure hardness. However, such screens may be necessary only in the most severe environments where the parts have a small margin, or for special cases such as radiation detectors.

4.2.3 Part categories. The categories into which parts may be segregated based on their various dose rate responses are:

a.	Hardness critical category 1M (HCC-1M)	Lot acceptance tests and/or hardness assurance screens required.
b.	Hardness critical category 1S (HCC-1S)	These parts may not require lot acceptance acceptance tests because they have sufficient design margin, but are included in the HCC-1 classification because they may be nonstandard parts, or may require special procurement from one or more specific manufacturers due to the particular process-related radiation characteristics of the manufacturers. HCC-1S parts may require occasional sample testing similar to that which may be done for HCC-2 parts, to assure that the process-related radiation characteristics do not change with time.
c.	Hardness critical category 1H (HCC-1H)	These parts would not require lot acceptance tests on the basis of design margin, but are included in the HCC-1 classification because they are hardness-dedicated parts. These parts are included in the design for the purpose of hardening. Protection diodes and circumvention detectors are in this category.
d.	Hardness critical category 2 (HCC-2)	These parts do not require lot acceptance tests, but may require occasional sample testing to verify that the manufacturing process has not changed significantly.
e.	Hardness noncritical (HNC)	These parts have such large design margins, or do not have a critical radiation failure criterion, so that testing is not required, even on an occasional basis.

4.2.4 Design margins. Design margins are used to categorize parts to determine the degree of control and testing that may be required. Two methods are proposed for classifying the parts, the design margin breakpoint method and the part categorization criterion method. Both methods require part radiation characterization test data to determine a design margin. The design margin is then compared to a numerical value specified by one of the two methods.

4.2.4.1 Design margin break point method (DMBP). The DMBP method (see 6.1.3 herein) is generally most useful for systems with moderate requirements. When the DMBP method is used, a single value of the DMBP is specified during the design phase. This number is the breakpoint between HCC-1M, where tests are required on each lot, and HCC-2, where tests are not required on each lot. In addition, a design margin which separates HCC-2 from HNC will also be specified.

4.2.4.1.1 Design margin break point value. Since the DMBP value is the breakpoint between categories 1 and 2. Increasing this value increases the confidence that can be placed in the HCC-2 part categorization. However, it also increases the number of HCC-1M part types that will require lot acceptance testing. Generally, it is cost-effective to set the DMBP value as low as practical within the risk factors established by the system requirements. The DMBP method is important for dose-rate hardness assurance because statistical failure distributions are not known for all effects, and the designer must rely more strongly on engineering judgment. A design margin breakpoint value will need to be specified on the basis of the best available information.

4.2.4.2 Part categorization criteria method. The PCC method (see 6.1.1 and 6.1.2 herein) is most often used for systems with severe requirements. However, one of the more important assumptions made in using the PCC method is that the failure response of the device may be characterized by a known, or perhaps a worst-case, statistical distribution. Before the methods used to determine the part categorization are presented, it should be pointed out that a significant portion of radiation test data seems to be best represented by the log-normal statistical distribution. (The log-normal distribution is nonsymmetrical, with a positively skewed tail.) The mean value for this distribution is the geometric mean, and the variance of the data is the geometric dispersion. To apply normal statistical calculations to log-normal data, it is first necessary to transform the data into a normal distribution space by taking the logarithm of the data. After the normal statistical calculations are completed, the antilogs must be used to transform the calculations back into the log-normal space (see 6.1.1 and 6.1.5 herein).

4.2.4.3 Design margin compromise. In addition to the DMBP and PCC values, the design developers may specify a level above the specification criteria requirements that is used to differentiate between unacceptable parts and those classified as HCC-1M. The value assigned to this number is based on several considerations. A small value may be desirable to minimize the number of part types categorized as unacceptable. However, too small of a value may result in an unacceptably high rejection rate during lot acceptance testing for part types with small design margin values. The value selected will be a compromise between these two factors.

4.2.5 Dose-rate statistics. Some dose-rate effects do not follow log-normal statistics. For example, some burnout data may follow a bimodal distribution (see 6.1.6 herein). Therefore, before these hardness assurance methods are applied, the statistics being used to define the hardness assurance tests must be verified through standard statistical tests. In some cases, a larger design margin the DMBP method may be used to compensate for distributional variations.

4.3 Worst-case analysis. The dose-rate environment produces a transient photoresponse in semiconductor devices which results in a variety of device effects, depending on the type of device. The design margin, on the other hand, is usually defined in terms of the ratio of the mean failure dose-rate to the specified level. Although the actual design margin may be defined in terms of a dose-rate margin, the actual failure occurs when a particular device parameter reaches some limit. This end-point electrical parameter failure value is called PAR_{FAIL} and is determined by worst-case circuit analysis.

4.3.1 Failure parameter criteria. Upset is a nondestructive transient effect that interrupts normal system operation. Circuit upset may or may not occur because of device photocurrent, depending on the circuit and piece-part response and recovery time. Hardening against upset can require circuit modification e.g., increasing circuit time constants, software modification, signal time sequencing, or piece-part replacement. Since dose-rate effects are often transient in nature, the actual failure parameter may not be one of the usually measured device parameters such as gain or saturation voltage. The dose rate effect may be an upset, change in output voltage, or even a device burnout. Table I gives a partial list of some common dose-rate effects for a number of device types.

4.3.2 Burnout analysis. Burnout analysis consists of determining the stress on the device and comparing that stress to the failure threshold of the device. However, burnout data in the dose rate environment is not usually readily available, and some procedure for estimating the burnout threshold must be used.

TABLE I. Typical dose-rate failure parameter criteria for several device types.

Part class	Parameter	Failure condition and comments
Diode	I_p = photocurrent	$I_p = I_{th}$ where I_{th} is the pulsed power damage threshold.
Transistor	I_s = saturation current	$I_s = I_{th}$ or
	I_{sp} = secondary photocurrent	$I_{sp} = I_{th}$
Linear ICs	Transient upset	$t_{rec} = t_{spec}$
	Burnout	$I_T = t_{th}$
	Latchup	Latchup cannot be handled in terms of a PAR_{FAIL}. Device ceases to respond.
Digital	Upset	ΔV_0 change in output V Upset may be handled in terms of noise margins, or simply in *terms of the dose rate which produces upset*
	Bit flip	Change of state in stored parameter.
	Burnout	$I_T = I_{th}$
	Latchup	Latchup cannot be handled in terms of a PAR_{FAIL}. Device ceases to function.

4.3.2.1 Failure estimation. At moderate dose rates, $(\dot{\gamma} < 10^{9}$ rads (Si)/s), burnout seldom occurs because of the energy in the pulse. Rather, burnout occurs because of the energy sources in the circuit, (power supplies, capacitors, inductors), releasing their energy in the device. The analysis then must consider the circuit current limiting, device susceptibility threshold and often will use the Wunsch-Bell equation (see 6.1.7 herein) or one of its modified forms (see 6.1.8 herein), to translate the threshold data to the time regime in question. If the device stress multiplied by the design margin is less than the expected failure threshold, the part is considered safe. If not, then device substitution, or circuit hardening techniques should be used.

4.3.2.2 Burnout data. Existing data bases usually exhibit a wide range of values in the burnout thresholds. These data bases are usually most useful for comparison of devices in the device selection process. For reliable burnout data, a number of factors such as the defined failure criterion, the test techniques, and the data analysis methods must be carefully examined for consistency with the application. If adequate documentation is not available with the data, the data base may be unusable for accurate burnout analysis, and new data may be required.

4.3.4 Latchup analysis. Latchup analysis consists of identifying devices which are susceptible to latchup. Some device technologies such as junction isolated integrated circuits are known to be latchup-prone. Other technologies may require formalized latchup analysis procedures (see 6.1.9 herein) to identify latchup paths. If latchup paths exist, then some action must be taken. Some of these actions have been discussed earlier, and consist of hardening features like part substitution, or system solutions (see 6.1.10 herein). Some technologies, such as SOS and SOI, are latchup free.

4.4 Design margins. There are several design margins which can apply to a system. As previously indicated, the dose-rate design margin is usually a ratio of a mean dose-rate threshold to a specified dose rate. However, there are some exceptions. Typical design margins are given below.

a. For circuits in which the failure probability increases with dose rate, the design margin is

$$DM_{\dot{\gamma}} = \frac{\dot{\gamma}_{MF}}{\dot{\gamma}_{spec}} \quad ,$$

where $\dot{\gamma}_{MF}$ is the mean dose rate for failure. An example of this design margin would be the case of upset in integrated circuits.

b. A subset of the first case would apply for circuits that incorporate circumvention in their design. In this case, the design margin would be

$$DM_{\dot{\gamma}} = \frac{\dot{\gamma}_{MF}}{\dot{\gamma}_{CIRC}} \quad .$$

c. For some cases, the failure results from a change in the relative circuit response time. The design margin in these cases may be defined in terms of the allowable transient duration. The design margin could be

$$DM_{\dot{\gamma}} = \frac{t(allowed)}{t(induced)} \quad .$$

The allowed transient duration could be a recovery time in digital circuits or a saturation time in linear circuits.

4.5 Data requirements. Radiation response data on devices are needed for various aspects of the design of a radiation hardened system. The requirements on data for the design hardening phase and the hardness assurance phase are somewhat different. These differences are related to the issue of part qualification and part acceptance.

4.5.1 Radiation characterization. Dose-rate response data are needed in the design hardening effort to aid in part selection and the determination of expected design margins. The characterization data may be obtained from existing data, or from new part characterization tests.

4.5.1.1 Burnout. Actual characterization measurements can be avoided if there exists a large body of data describing the dose-rate response of the devices. However, extreme caution must be exercised when existing data are used. Since most dose-rate effects are related to device geometry, diffusion length, doping, etc., assurance must be obtained that the data being used do in fact apply to the device in question.

4.5.1.1.2 Existing data sources. Existing data sources for burnout data may be considered for use. However, there are a variety of ways in which burnout data may be taken. The test pulse duration and shape, the test circuit, the definition of failure, and the sources of devices are all variables which may affect the data. Burnout threshold data may be useful, provided that the design margin is large enough to make the devices HCC-2 or HNC.

4.5.1.1.3 Latchup. Latchup can be a low probability failure mode in latchup-susceptible devices, and no amount of existing data can establish the latchup susceptibility of a part type with confidence. Latchup is lot sensitive, and existing data generally are not useful except to demonstrate that a particular device has a significant latchup problem.

4.5.1.1.4 Piece-part photocurrent data. The use of piece-part photocurrent data is frequently limited in upset analysis to comparison of circuits and devices as a first-cut screen to identify critical circuits that require detailed analysis and further test data. Existing piece-part photocurrent data often must be interpolated or extrapolated because the radiation levels or pulsewidths used to obtain the data are not the same as those of the specified environment. Extrapolation of photocurrent data to higher radiation levels can lead to large errors because effects become nonlinear (e.g., the device may saturate).

4.5.1.2 Characterization tests. Characterization measurements are made on samples of parts to estimate the radiation response of the population of parts. The sample set consists of piece parts of a single part type selected from a procurement lot. It is important to assure that a variety of date codes be represented in the sample in order to obtain a representative device response (see 6.1.11 herein). Several situations exist.

4.5.1.2.1 Upset testing. Upset testing is almost always nondestructive. Therefore, an upset threshold test on 100 percent of the devices could be performed, provided that only a small number of state vectors are required to be tested. For large-scale integrated circuits, the number of state vectors which need to be tested may preclude a 100 percent test because of potential total dose damage to the device, test time and cost. In these cases, the upset threshold must be found on a sample basis.

4.5.1.2.2 Burnout threshold. Burnout threshold measurements are destructive tests. Therefore, sample measurements must be made. The principal difficulty in burnout characterization is that threshold data are quite variable, the tests are time consuming, and since tests are usually done on small samples, good statistical analysis is not available (see 5.3.2).

4.5.1.2.3 Latchup. Latchup is a problem which cannot be solved by sampling, since latchup can be a low probability failure mode. Therefore, sample tests are usually inadequate to determine the extent of the problem. As a result, latchup cannot be handled by statistical inference.

4.5.1.3 Sample sizes. It is important, from statistical considerations, that as many devices as practical be used for radiation characterization measurements (see 6.1.12 herein). A good statistical test would include at least 25 parts, and more would be better. The sample should come from several lots. An absolute minimum would be five parts, with such a small number being used only when the parts are difficult to obtain or the tests are very expensive. A small number of parts could lead to a poor and possibly erroneous characterization. Furthermore, since the criteria for categorizing parts may depend on statistical considerations, the use of a small number of parts may result in devices being categorized as HCC-1 (lot acceptance test required) simply because of wide statistical uncertainties. This situation can lead to the requiring of large design margins, and perhaps greater expense. It is worth noting that a small sample size may turn out to be an "expensive economy."

4.5.1.4 Measurement of stress to failure. The recommended procedure for characterization measurements is to measure the threshold dose rate at which the dose-rate effect occurs. Many test methods have been written describing radiation test procedures. A listing of some of these procedures is given in Appendix B.

4.5.1.4.1 General test procedures. The general test procedure varies, depending on the effect being measured. However, in almost all cases it is the threshold dose rate at which the dose-rate effect occurs, which is to be measured. The exception to this rule is data taken for burnout effects. This exception will be discussed later.

4.5.1.5 Example of upset data. An example of data for CMOS 16K random access memories is shown in table II. The data shown are for loss of data measurements performed at a linear accelerator. These data are presented as an example of the calculations described in the previous section, and should not be used for design information. A log-normal cumulative plot of the data is shown on figure 2, indicating the well-behaved distribution of this particular data set. A similar plot would need to be made for each data set in order to assure that the statistics used do, in fact, apply to the data in question.

4.5.1.5.1 Data points. The data points representing the lowest upset value for the dose rate have been least square fit for the analysis. Using the lowest upset values may be adequate for data of sufficient quality, where the difference between the highest nonupset dose rate and the lowest upset dose rate is only a few percent (~25 percent). In other cases, a maximum likelihood estimate could be used (see 6.1.13 herein).

4.5.1.5.2 Log-normal statistics. The cumulative plot of figure 2 indicates that the distribution of these data is approximately log-normal. Therefore log-normal statistics will be assumed to be justified for use for hardness assurance on this device. The log-normal mean and standard deviation are calculated in table II for use in this document. (These parameters are defined in 3 herein.)

4.5.2 Nonstatistical problems. Some dose-rate effects cannot be analyzed statistically. For example, latchup sometimes has such a low occurrence rate that the gathering of statistics about the stress to failure would be impractical. Therefore, in the case of latchup, a less rigorous hardness assurance approach is often used for devices that are latchup prone. The procedure generally follows one of the following techniques:

a. Latchup screens.

b. Latchup analysis.

c. System solutions.

4.5.2.1 Latchup screens. When four-layer paths exist in devices, the question of latchup must be considered. It has been suggested that if the beta product of the four-layer path could be determined, latchup could be handled statistically. However, insufficient data exists to qualify this technique, since parasitics are involved and quantification is elusive.

4.5.2.1.1 Imposed screens. Latchup screens are often imposed to find latchup-free devices. These screens are designed to nondestructively test 100 percent of the devices in an ionizing radiation source (see 6.1.14 herein). Recently, 100 percent screening of parts has come under criticism on the basis that the screen may overstress the parts, thus creating latent defects and impacting device reliability. This postulate has not yet been experimentally justified. All devices which latch are discarded. Problems associated with this technique are discussed in 5.2.2 herein.

TABLE II. Loss of data parameter measurement.

Device Serial Number	All 1's			
	No Upset		Upset	
	$(\dot{\gamma})$	$\ell n(\dot{\gamma})$	$(\dot{\gamma})$	$\ell n(\dot{\gamma})$
1	8.00 E6	15.89	8.57 E6	15.96
2	7.14 E6	15.78	8.29 E6	15.93
3	8.29 E6	15.93	9.71 E6	16.09
4	8.29 E6	15.93	8.86 E6	16.00
5	1.00 E7	16.12	1.03 E7	16.15
6	1.00 E7	16.12	1.11 E7	16.22
7	1.09 E7	16.20	1.11 E7	16.22
8	1.00 E7	16.12	1.14 E7	16.25
9	1.06 E7	16.18	1.14 E7	16.25
10	1.17 E7	16.28	1.29 E7	16.37
	Avg. $\ell n(\dot{\gamma})$ =	16.06	Avg. $\ell n(\dot{\gamma}_{FAIL})$ =	16.14
	Std.Dev. $^{S}\ell n(\dot{\gamma})$ =	0.16	Std.Dev. $^{S}\ell n(\dot{\gamma}_{FAIL})$ =	0.15

4.5.2.2 Latchup analysis. A latchup analysis procedure (see 6.1.9 herein) has been developed for bipolar circuits to aid in the latchup assessment of circuits. The purpose of the latchup analysis procedure is to determine whether the device is latchup free, by using an analytical technique. This procedure attempts to identify all the four-layer PNPN paths in the device. By use of this procedure, one can determine if four-layer paths exist, and if they are biased correctly for latchup, the device will not latchup. It should be noted that such analyses are complex and involve considerable time in acquiring the necessary device-design data to perform the analysis.

4.5.2.3 System solutions. Finally, latchup can be handled effectively at the system level by a variety of methods. These methods are not the subject of this document, and thus are not discussed in detail here. However, some of the more effective techniques are:

a. Power management, whereby the power to the device is momentarily interrupted, thus interrupting latchup.

b. Current and voltage limiting, where the applied bias and the allowable current are held well below those required for latchup.

4.5.2.4 Piece part solutions. The best solution to the latchup problem is to use devices which are not latchup susceptible whenever possible. Three means of avoiding latchup at the device level are:

a. Dielectric isolation, where no more than two active junctions are allowed within an isolated region, silicon on sapphire or silicon on insulator substrates.

b. Process controls to prevent latchup, which reduce the parasitic gains of the four-layer paths to extremely low values. These controls may involve gold doping, neutron radiation, epitaxial layers on highly doped substrates.

c. Analysis which demonstrates that any four-layer paths that may exist cannot latch because of bias or circuit conditions.

4.6 Lot acceptance testing. Hardness assurance acceptance tests are performed on devices during the production phase of a program. These tests are usually performed on samples from procurement lots of devices in order to assure that the devices procured during production have the same radiation performance as indicated in the characterization tests. Acceptance testing will be discussed in 5 herein.

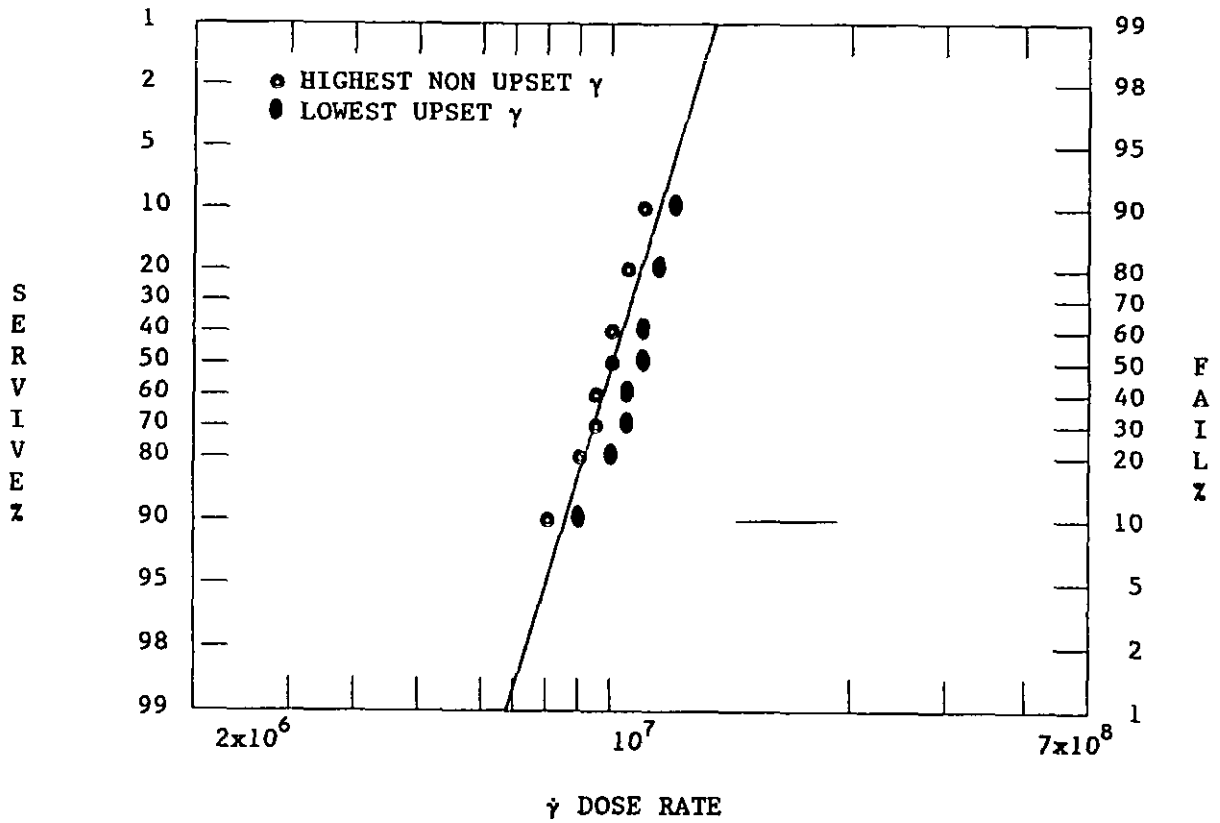

FIGURE 2. Cumulative log-normal plot of upset dose rate.

5. HARDNESS ASSURANCE

5.1 Hardness assurance. Hardness assurance (HA) is the application of methods and procedures during the production phase of a system to ensure that the system retains the radiation hardness which it was designed to have. Although the principal application of hardness assurance is in the production phase, it is necessary to consider HA during the design phases of a program if a cost-effective system is to be obtained. Hardness assurance begins in the design phase with definition of the system requirements, radiation characterization of the piece-parts, calculation of the required design margins and the categorization of semiconductor parts.

5.1.1 Design margin. The design margin approach for part categorization is used to determine if hardness assurance lot acceptance testing is required for a particular part type. The two methods used for this categorization are the design margin break point (DMBP) method and the part categorization criteria (PCC) method. Both methods require part characterization data to determine the design margins.

5.1.2 Design margin break point. DMBP is generally used for systems with moderate requirements, and in cases where dose-rate responses of the devices are well understood, or at least are bounded. In this case, the calculated design margin for each piece-part is compared to specified breakpoint, and based on this comparison, the part category is chosen.

5.1.3 Part categorization criteria. PCC applies in all cases where the statistical distribution of failure is known, and is generally used in systems with severe requirements on part survivability. Sometimes a combination of the two methods can be used; that is, DMBP is used to categorize less sensitive parts, and the PCC value is used for the more sensitive parts.

5.1.4 Unacceptable parts. In any application of these hardness assurance methods, a value must be specified which will be used to separate unacceptable and HCC-1 parts. The value must be based on several considerations, such as number of parts rejected, part availability and cost. Table III illustrates this using a value of 2.

5.1.5 DMBP method. The DMBP method is often specified for systems with moderate requirements with respect to the device response levels. The DMBP values are sometimes based on statistical baseline, but are more often based on good engineering judgement, threat specification levels and system considerations. The first DMBP value is the break point between HCC-1M, where acceptance tests are required on each lot, and HCC-2, where tests are not required on each lot. DMBP provides a qualitative level-of-survival probability and confidence level, based on past generic response and engineering judgement. Table III shows the relationship between the break point values. The second DMBP value is the breakpoint between HCC-2 and HNC.

TABLE III. Relationship between dose-rate DM and DMBP value.

Dose rate DM	≤ 2	≤ DM	≤ DMBP (1) Value	≤ DM	≤ DMBP (2) Value	≤ DM
Part is unacceptable		HCC-1M part; lot acceptance testing is required		HCC-2 part; lot acceptance testing is not required		HNC

5.1.6 PCC method. The PCC method (see 6.1.1 and 6.1.2 herein) is generally required for systems in which stringent requirements are placed on part types. When PCC is used, it is necessary to calculate the PCC values based on the characterization data. The PCC data are used primarily to differentiate between HCC-1 and HCC-2. A second PCC could be calculated using a smaller allowed failure probability (or a breakpoint could be chosen) to separate HCC-2 parts from HNC parts. Table IV shows this relationship. When the part is judged unacceptable, the corrective action indicated in 5.1.3 should be considered.

TABLE IV. Relationship between dose-rate DM and PCC value.

Dose rate DM ≤ 2	≤ DM	≤ PCC (1) Value	≤ DM	≤ PCC (2) Value	≤ DM
Part is unacceptable	HCC-1M part; lot acceptance testing is required		HCC-2 part; lot acceptance testing is not required		HNC

5.1.6.1 PCC calculations. Before the method used for determining the PCC value is presented, a discussion of the factors used in the calculations is in order. The discussion will include the variability of the dose-rate failure values obtained during characterization, a confidence factor and the required survival probability.

5.1.6.2 Variability. The variability of the data is represented by the standard deviation, s, and is calculated using the $\dot{Y}_{FAIL}$ values described in 4.2.4. Because the log-normal distribution is assumed, $s_{ln}(\dot{Y}_{FAIL})$, which is the standard deviation of the logarithm of the $\dot{Y}_{FAIL}$ values, is calculated as follows.

$$s_{\ell n}(\dot{Y}_{FAIL}) \equiv \left(\frac{1}{n-1} \sum_{i=1}^{n} [\ell n(\dot{Y}_{FAIL_i}) - \overline{\ell n(\dot{Y}_{FAIL})}]^2 \right)^{1/2},$$

where $\dot{Y}_{FAIL}$ is the dose rate resulting in failure for the i^{th} device, and n is the sample size.

5.1.6.3 The level of confidence and survival probability. The level of confidence and the survival probability are introduced into the calculations by multiplying $s_{\ell n}(\dot{Y}_{FAIL})$ by the one-sided tolerance limit factor K_{TL}, which is selected from a table of one-sided tolerance limit factors (see appendix C). This factor is a function of sample size n, survival probability P_{DIST} and confidence level C. For example, 90 percent confidence in 99 percent probability of survival means that if the characterization test were repeated many times on different samples from a lot, 90 percent of the time 99 percent of the $\dot{Y}_{FAIL}$ values would be equal to or greater than the mean less K_{TL} times the standard deviation s, or $\overline{\ell n(\dot{Y}_{FAIL})} - K_{TL}\, s_{\ell n}(\dot{Y}_{FAIL})$, for a log normally distributed variable. The PCC value is calculated from the following relationship.

$$PCC = \exp K_{TL}\, s_{\ell n}(\dot{Y}_{FAIL}) .$$

5.1.6.4 Increasing P_{DIST} and C, and consequently K_{TL}. Increasing P_{DIST} and C, and consequently K_{TL}, increases the PCC value and the cost of the hardness assurance program, since increasing the value of PCC increases the number of part applications that will be categorized as HCC-1M, requiring expensive lot acceptance testing. Increasing the sample size n generally will increase the cost of the characterization test. However, this added cost may be more than offset during the HA phase of the program, since increasing the value of n results in a lower value of K_{TL} and hence a lower PCC. This in turn may reduce the number of part types requiring lot acceptance testing. As can be seen, the values of P_{DIST}, C and n selected are a tradeoff between the level-of-hardness assurance desired and the amount of funding available for the HA program. The values of P_{DIST}, C and n Should be approved by the SPO when the PCC method is used.

5.1.6.5 Part type HCC-2. A part type classified as HCC-2 does not require routine lot acceptance testing. However, when the dose-rate margin approaches the PCC value, a sample test should be conducted periodically during parts procurement. It should be noted that a value of 10 is often used as the breakpoint value for HCC-2 when using the DMBP method.

5.1.6.6 Dose-rate upset testing. Nondestructive tests such as dose-rate upset testing may be performed on a 100 percent screening basis for parts which have been categorized as HCC-1. Table V indicates the possible test action which may be required.

TABLE V. Possible testing requirements.

	HCC-1	HCC-2
Upset	100% screen	Periodic lot screen
Burnout	Sample test	Occasional sample test
Latchup	100% screen	Not required

5.1.7 Use of the PCC method. If a system has stringent requirements, or if the parts used in the system have failure levels close to the specification level, then a separate decision must be made about the risk to be taken for each part type used. Sometimes, only a few part types are mission critical, and cannot be allowed to fail. Often, certain memories used in the system may not be allowed to upset or to lose data through the radiation event. For these parts, an estimate of the survival probability and the confidence in survival are essential for design hardening.

5.1.7.1 The reason for using the PCC method. The reason for the use of the PCC method is that the calculated design margin is usually lowered from the value used in the DMBP method, since the margin is based on the actual device performance, and not on a worst-case estimate of the performance of a number of device types.

5.1.7.2 An example. Let us assume that the memory used on figure 2 is used in a system in a moderate environment. Let us further assume that the requirements for the part are described in table VI.

a. The first quantity required for the calculation is the dose-rate design margin. This is determined from the data of table II and the upset level specification.

b. The mean failure level is given in section 4.2.5 as $\dot{\gamma}^{MF} = \exp \ell n(\dot{\gamma})$.

c. From the data in table 2, $\dot{\gamma}_{MF} = \exp(16.14) = 1.02E7$.

d. With a the specified threat level of 5E6, the dose-rate design margin is

$DM_{\dot{\gamma}} = 1.02E7/5E6 = 2.05$.

e. The part categorization criterion, PCC, is obtained from 5.1.2. The one-sided tolerance factor, K_{TL}, is obtained from appendix C; for the appropriate sample size (N = 10), the survival probability (P = 0.9999), and the confidence level (C = 0.9). Caution must be exercised when extrapolating data to extremely high probability levels.

$$PCC = \exp K_{TL} s_{\ell n}(\dot{\gamma}_{FAIL})$$

$$PCC = \exp(5.538 \times 0.15) = 2.3.$$

f. Since the PCC value is larger than the DM, the part is categorized as HCC-1M and lot acceptance tests must be performed.

TABLE VI. Requirements at part location.

Specified threat level	5 E6 rads(Si)/s
Required-survival probability	0.9999
Required confidence level	0.9

5.2 Hardness assurance requirements. The various techniques which can be used for hardness assurance have now been discussed. This section will provide some guidance on how to apply some of these techniques to various systems.

5.2.1 Upset hardness assurance. Either the DMBP or the PCC method could be used for hardness assurance decisions, depending on the required probability of survival and the device technology used. Upset testing may often lead to an adequate statistical determination of thresholds for failure. One, therefore, has the option to use a number of different hardness assurance techniques in the application of the PCC and DMBP methods. One can select from:

a. Device selection.

b. Design modification.

c. 100 percent screen.

d. Sample testing.

e. System solution.

5.2.1.1 100 percent screening. For systems requiring high confidence of survival, a 100 percent screen may be used to assure the upset survivability of the device with greater confidence. A 100 percent screen can be an effective technique for integrated circuits at small-to-medium levels of integration. For higher levels of integration, a statistical approach may be used, since the number of state vectors required to be tested may preclude a 100 percent screen. The cost of a 100 percent screen can be large, and one must make a tradeoff between the cost of testing each device and the required survivability of the system.

5.2.1.2 Sample testing. For systems with moderate requirements, the DMBP technique may be the most cost-effective method of achieving the desired confidence in survival. For cases where the design margin is small, the PCC method may be used to determine if lot acceptance tests may be required.

5.2.1.3 System solution. In most cases, a system-level solution for upset can be used. The circuits can be designed to be upset tolerant, and would be reset after the pulse of radiation. Devices less sensitive to radiation can be substituted for radiation "soft" devices. In the final analysis, a combination of techniques provides the best solution to the upset hardness assurance problem.

5.2.2 Latchup hardness assurance. Since latchup may have a low probability of occurrence, hardness assurance for latchup presents a unique problem. There are very few cases where sufficient statistical data exists to apply the PCC hardness assurance method. In moderate environments, where the dose rate environment is significantly lower than the expected latchup thresholds of the devices, the DMBP method may be used. In any case, alternate hardness assurance techniques must be used. The only techniques available to be used are the following:

a. Device selection.

b. 100 percent screen.

c. System solution.

5.2.2.1 Hardness assurance for latchup. Hardness assurance for latchup is best solved by part substitution or by a system-level solution. Part substitution implies that parts which are not latchup susceptible are substituted for parts which are latchup prone. There are a number of ways by which latchup-free devices are found. Some of these ways are discussed below.

5.2.2.1.1 Device construction. The use of special processing methods, such as dielectric isolation, buried layers, gold doping, etc., are techniques which are used to prevent latchup. These techniques either eliminate four-layer paths or assure that the parasitic gains of the devices are too small to sustain latchup.

5.2.2.1.2 Latchup screens. The use of latchup screens attempts to find devices which latch by using a nondestructive radiation screening test. Devices which latch are eliminated from use in the system. There are several significant problems with the use of latchup screens; these will be discussed later.

5.2.2.1.3 Latchup analysis. Latchup analysis is an attempt to find latchup-prone devices through the analysis of the layout and processing rules used in the device manufacture. It is usually assumed that devices that have four-layer paths will not latch if the current source supplying the path is insufficient to support latchup. Since the four-layer paths are parasitic, one must perform a careful analysis to ensure that the biases and current sources that are present in the nonradiation environment are in fact the correct current and bias sources that are supplying the path during the dose-rate irradiation.

5.2.2.2 Cautions - latchup. There are a number of precautions which need to be considered when deciding on latchup hardness assurance techniques. Some of these precautions are discussed below.

5.2.2.2.1 Latchup screens. Most latchup tests are performed using a Linac or a flash x-ray facility. These tests are usually made at a fixed dose, approximately 500 rads(Si), in some specified test configuration. There are a number of problems with this kind of test procedure.

a. The first uncertainty is the design of the test configuration. It is necessary to determine the worst-case conditions for the test, and to bias the device properly for the test. The latchup analysis procedure is the preferred way to arrive at these worst-case conditions. An arbitrary choice of biases and test configuration can only lead to uncertainty in the test results.

b. LSI circuits pose a more complex problem. The problem of proper selection of test vectors for the latchup screen is extremely complex. It can be made on the basis of internal rail-span collapse analysis, internal node fan-out and functionality. These circuits may contain more output states than can be practically monitored, and an evaluation of the application of the device in the system in which it is used is one way that the test vectors may be determined. This, of course, leads to uncertainties in the results of the screening procedure. In these cases, it is often better to power strobe or power interrupt upon detection of a radiation pulse.

c. Finally, it is well recognized that latchup in integrated circuits is temperature dependent. This is because the condition of latchup depends on the magnitude of the gain of parasitic transistors in the integrated circuit, these gains increase with temperature dependent, and may vary by factors of three to four over the operating temperature range. A device which does not latch in a room temperature test may latch in a test at the maximum operating temperature. Therefore, the screen must be performed at the maximum device operating temperature in order to be valid.

5.2.2.2.2 Latchup windows. The difficulties of latchup screening are exacerbated by the existence of latchup windows some technology types. Thus, prior to screening a careful characterization must be accomplished to identify this phenomenon, if it exists.

5.2.2.2.2.1 Latchup window phenomenon. The latchup window phenomenon has been seen in CMOS devices. In particular, the CD4047, CD4061 and the CD4094 have been observed to have latchup windows. However this has not been shown to be a widespread issue. There is no reason to believe that the latchup window problem is limited to CMOS devices.

5.2.2.2.3 Latchup analysis. Latchup analysis is a useful tool in the identification of latchup in devices. The latchup analysis procedure details the requirements and methods to perform the analysis to achieve reasonable confidence in the result. However, the application of the technique requires detailed knowledge of the design rules for the device, and the acquisition of layout information for the device processing. This information is difficult to get.

5.2.2.2.3.1 Objectives of latchup analysis. The objective of the latchup analysis procedure is to identify all four layer paths in the device and to make a judgement about whether or not the paths will latch. Obviously, if no paths exist, the device is latchup free. However, if paths are found in the device, the procedure seeks to determine the susceptibility of the paths.

5.2.2.2.4 Suggested procedure. A reasonable procedure to follow for latchup hardness assurance is described below for devices.

a. The process begins with device selection. The devices are subjected to a analysis to determine whether or not four layer paths exist. If no paths exist, a high-confidence, latchup-free design can be assured.

b. Should four layer paths exist, two options are available. The part may be replaced and the process repeated, or the circuit design may be altered. Should the analysis again determine that a four layer path exists that is properly biased for latchup, two options are possible. The parts may be screened to test for latchup occurrence using test conditions determined from the analysis. This procedure may result in moderate confidence in a latchup-free system. Alternately, a system solution, such as circumvention, may be used to obtain a high confidence, latchup-free design. However, power must be removed quickly, within a few tens of microseconds, to prevent burnout in devices.

c. Should a four-layer path exist, and should the latchup analysis demonstrate that the path is not biased correctly for latchup to occur, one can terminate the process with low to moderate confidence that the system is latchup free. However, the analysis should include the effects of radiation and electrical transients to ensure that the latchup structure cannot be activated during such events. This approach may be feasible and cost effective for the kinds of systems where latchup may be tolerated and operation manually restored.

d. Alternately, one may improve the system through the use of latchup screens and system solutions or both. This flow is diagrammed on figure 3.

5.2.3 Burnout hardness assurance. Burnout in the dose rate environment may take on more than one form. The most common failure is junction burnout, occurring as a result of the dose rate radiation. Another burnout mechanism can be the failure of the metallization. Hardness assurance techniques for controlling these effects are considered, at present, to be only tentative and unproven. The matter of burnout in the dose rate environment is still the subject of research, and a complete characterization of the mechanisms is not yet available.

5.2.3.1 Method of choice. The most reasonable choice of a hardness assurance method is the DMBP method. However, the calculation of a design margin break point is complicated by the fact that all burnout conditions are not fully understood. As a result the hardness assurance techniques available are the following:

a. Device selection.

b. Current limiting.

c. System solutions.

5.2.3.1.1 Application of the techniques. These techniques are used to achieve a design margin which is sufficiently large to assure survivability. Since uncertainty exists in the actual burnout threshold of devices, a great deal of judgement must be used in the application of the techniques.

5.2.3.1.1.1 Device selection. The use of devices which have higher burnout thresholds is a useful hardness assurance technique. However, since little data are available on burnout in the dose rate environment, pulsed power data are often used to compare the relative hardness of devices. Pulsed power data may provide a meaningful measure of relative hardness for discrete devices and small scale integrated circuits. However, larger scale integrated circuits may have internal failure modes in the dose rate environment which may not be measured by pulsed power techniques.

5.2.3.1.1.2 Current limiting. The most effective hardness assurance technique for burnout hardness is the technique of current limiting. The purpose of current limiting is to prevent any current sufficiently large to cause burnout from flowing into the terminals of the devices. Power supplies, capacitors and input/output terminals are protected with current limiting resistors. A rule which is often used is to provide approximately one ohm of resistance per volt to provide current limiting for all lines connected to an energy source. Input and output leads can be protected to levels to prevent pulsed power burnout at those terminals. Current limiting resistors added for burnout protection are classified HCC-1H. However, one understandable consequence of current limiting is to lower the device upset level since the voltage provided to the device is reduced by the surge I_{pp}.

5.2.3.2 Burnout hardness assurance - cautions. The question of hardness assurance for burnout in the dose rate environment is an extremely difficult issue. The principle difficulty is the fact that very little burnout data exists for devices in the dose rate environment. In fact, available burnout data for devices is often performed using pulsed power techniques, and comparisons are made on the basis of that data.

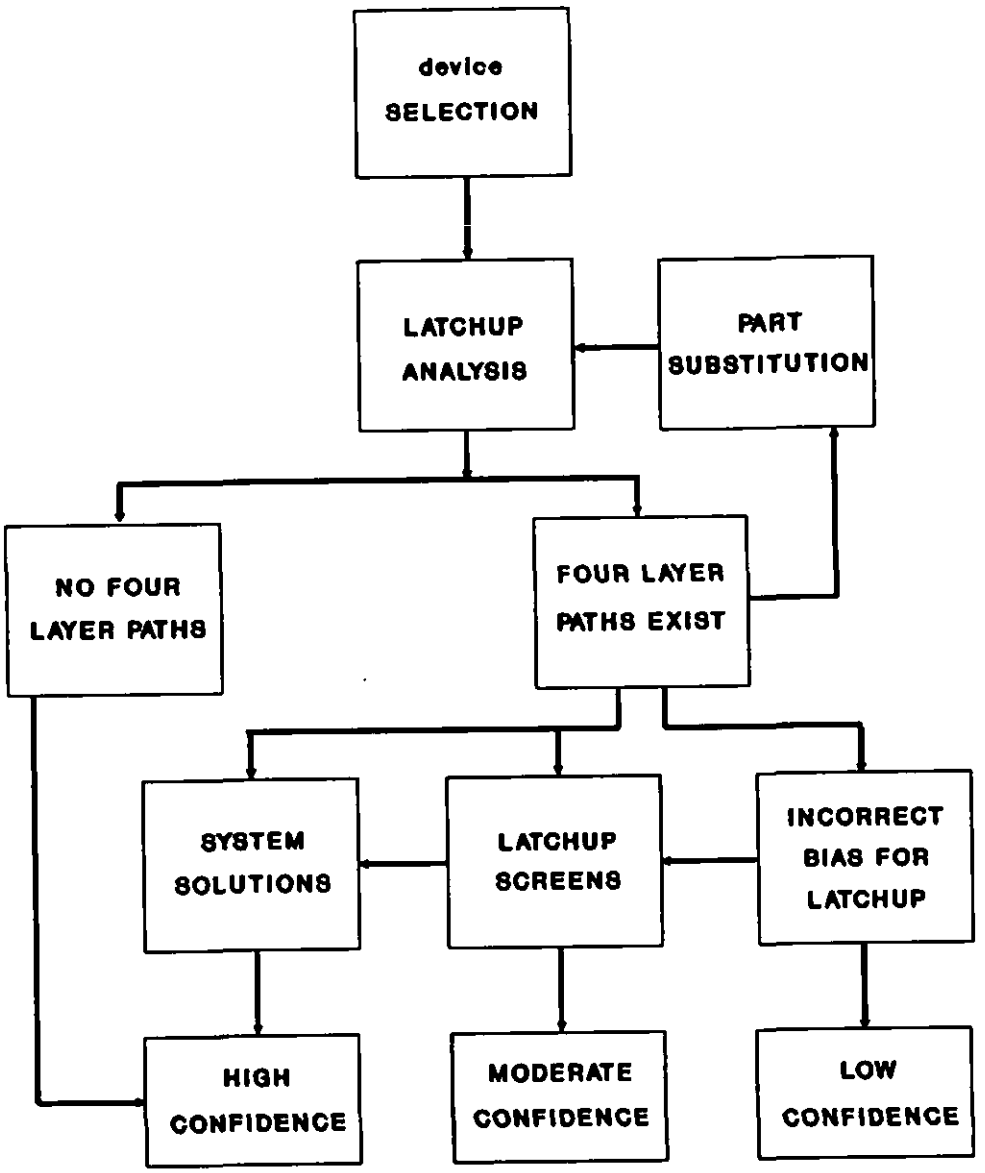

FIGURE 3. Latchup flow diagram.

5.2.3.2.1 Unanswered questions. Unfortunately, the vast majority of the existing data addresses discrete devices. A further complicating factor is that several significant unanswered questions have arisen concerning the existing data. Some of these questions which cause concern are listed below.

a. Some devices do not conform to idealized models for device burnout response.

b. The distributions of burnout response do not always conform to expected statistical response.

c. The burnout response of integrated circuits in dose rate environment may be different than the response predicted on the basis of discrete device pulsed power data.

d. The criterion for burnout may differ between devices. No standard test methods exist.

e. Synergistic effects affecting burnout are not completely understood.

5.2.3.2.2 Uncertainties. As a result of these uncertainties, burnout hardness assurance has not been well developed. System hardening techniques will need to be used until many of the unanswered questions have been resolved. Some of these uncertainties are discussed in the following sections in order to provide an understanding of the magnitude of the problem.

5.2.3.2.2.1 Idealized burnout models. In many instances, the catastrophic effects of current or power stresses on devices are the significant failure mode for the system. However, the methods used to analyze and obtain design data for the systems do not lead to a great deal of confidence in the analysis.

5.2.3.2.2.1.1 Contributing factors. The power required to burn out a semiconductor junction depends on a variety of factors. Some of these factors are the physical geometry of the device, the impurity profile, the bulk and contact resistance of the device, the polarity and intensity of the applied stress, and a variety of other factors. The point is that although a large number of factors which contribute to the failure of a device have been identified, the burnout problem in devices is not yet completely understood.

5.2.3.2.2.1.2 Unanswered questions. Much work has been done to further our understanding of the phenomenon. Some of the most important unanswered questions are:

a. What are the proper test methods for determining failure thresholds and minimizing the scatter in the data?

b. What is the proper statistical distribution which describes the variation of burnout data with stress?

c. Are there any measurable, nondestructive, screening parameters which can indicate a device with a low failure threshold?

5.2.3.2.2.1.3 Analysis. One of the most common burnout models used in analysis is the Wunsch-Bell power model (see 6.1.7 herein). This model is an engineering approximation to the physics of the idealized pulsed power burnout phenomenon as it is presently understood.

5.2.3.2.2.1.4 Initial design. Initial design of circuitry is usually based on burnout threshold data previously acquired, or new test data obtained specifically for the program. Typically, a sample of devices is tested to provide characterization data where they do not already exist. The tests are usually performed on electrically equivalent unscreened parts.

5.2.3.2.2.1.5 Failure threshold. The failure threshold is usually determined by step-stressing the device using single electrical pulses of increasing power, but of fixed pulsewidth. The device is characterized after each pulse to detect any damage.

5.2.3.2.2.1.6 Power level. The power level increase between pulses becomes a critical factor in the tests. A factor of two increase between pulses is not unusual. Therefore, the uncertainty in the threshold may be as much as 3 dB, simply due to test techniques. The time to burnout may be somewhat less than the pulsewidth of the driving pulser.

5.2.3.2.2.1.7 Time regimes. For time regimes between tens of nanoseconds and a few microseconds, it is noted that the power required to burn out a junction in reverse breakdown is $K/t^{1/2}$, directly from the Wunsch-Bell equation. This power is absorbed in the junction and bulk resistance giving a current of

where $$I_{TH} = -V_{BD} + (V_{BD}^2 + 4R_B K/t^{1/2})^{1/2} ,$$

R_B is the device bulk resistance.

V_{BD} is the junction breakdown voltage.

K is the Wunsch-Bell damage constant.

t is the rectangular pulsewidth.

Measured values of K are recommended to be used. However, when quality data are not available, the values of K are usually derated according to some derating scheme. One such scheme is shown in table VII.

TABLE VII. Derating factors for Wunsch-Bell damage constants.

Source	Derating
Reliable, well-documented data	1/3
Similar part test data	1/10
Calculated data	1/50

For parts which are characterized for the system in which they are to be used, another modification of the Wunsch-Bell equation is often made. The test data are least-squares fit to the equation:

$$P = At^B,$$

where P is the power, t is the pulse duration and A and B are constants found by the least-squares fit. Then this curve is used to find the failure threshold at the expected pulsewidth. Once the derated current is found and the damage threshold is determined, then the circuit currents are limited to yield a desired design margin.

5.2.3.2.2.1.8 Basic assumptions. All of the approaches presently used make certain basic assumptions and use similar extrapolation methods. For example, the Wunsch-Bell engineering model is commonly used. It is often necessary to extrapolate the burnout data to pulsewidths of interest, and the simple power law seems to be a convenient way to perform this extrapolation.

5.2.3.2.2.1.9 Analysis techniques. There are a number of areas which must be discussed in assessing these analysis techniques:

a. Statistics of the burnout threshold.

b. Extrapolation using the Wunsch-Bell power law.

c. Combined environmental effects.

5.2.3.2.2.2 Statistical analysis. Burnout testing of devices has yielded very little in the way of information on the statistical distributions describing burnout data. If the statistical distribution is known, derating part data for the statistical uncertainties resulting from small sample data is a straightforward application of confidence bounds. The techniques outlined previously using one-sided tolerance limits can be modified to whatever distribution is used. On the other hand, without knowledge of the statistical distributions, any derating scheme is subject to question.

5.2.3.2.2.2.1 Statistical distribution. A number of authors have attempted to study and describe the statistical distribution of burnout data. Typical of these efforts are the works of Egelkrout and Alexander et al.

5.2.3.2.2.2.2 Egelkrouts study. The most commonly used distributions are the normal and log-normal distributions. Egelkrout set out to examine the lot-to-lot variability of burnout data, and attempted to show that existing data analysis methods and the statistics used result in inadequate design margins (see 6.1.6 herein). He also tested several trial distributions against existing data to determine the proper statistical distribution. He postulated that burnout data may follow a Weibull distribution rather than the usual log-normal. Egelkrout does, in fact, show that the statistical problem is not yet solved. Perhaps more careful test procedures and use of confidence limits in the statistical extrapolation may result in a more realistic estimate of useful margins.

5.2.3.2.2.2.3 Alexanders study. Alexander, et al., attempted to develop failure threshold information by testing large numbers of transistors (see 6.1.19 herein). A number of transistor topologies were used in the experiment to provide the variety of shapes and sizes commonly used in aeronautical systems. A number of common statistical distributions were tested to determine which distribution would be most useful for failure threshold analysis. They found that no single distribution was universally applicable to their data.

5.2.3.2.2.2.4 Conclusion. The point to be drawn from this is that the use of any statistical procedure based on the failure threshold for devices leads to some degree of uncertainty. Without an adequate statistical description, the extrapolation from sample data cannot be made with confidence. Most often, what is done is that a particular distribution is judged to be acceptable from an engineering point of view and is used on that basis.

5.2.3.2.2.2.5 Burnout threshold variability. It may be useful to examine the burnout threshold variability from a nonparametric perspective. The designer may wish to know the number of standard deviations from the mean which are required to bound the failure threshold. If the failure threshold can be bounded to within an acceptably small limit, then a suitable design margin can be chosen.

5.2.3.2.2.3 Pulsewidth dependance. Burnout data are most often measured using one or two stressing pulsewidths. Should the pulsewidth of interest not be the same as the measurement stress, the data will have to be extrapolated, or interpolated in order to provide failure thresholds at the required pulsewidth.

5.2.3.2.2.3.1 Idealized power laws. Extrapolation using the idealized power laws can lead to errors since the idealized power laws apply only to limited time regimes or pulse widths. Extrapolation to pulsewidth outside of the region of applicability can lead to very significant errors. In addition, the uncertainty of the data on which the extrapolation is made contributes to the error.

5.2.3.2.2.4 Combined environments. There is some concern about the combined effect of nuclear environments, particularly in the area of burnout. There may be a combined effect should the dose-rate effect occur simultaneously with the incidence of an electrical overstress. This problem has been studied by some researchers, with varying degrees of success. These studies indicates that current limiting of devices serves to effectively control combined effects for most digital and analog devices. High power devices, where current limiting is difficult, may be subject to combined effects, and testing in the dose-rate and pulsed power combined environment may be required.

5.3 Lot acceptance testing. During the production phase of a program, it is assumed that the parts which are to be used have been characterized and categorized during the design phase. The most cost-effective approach to piece-part hardness assurance is to determine the part requirements during the design phase, and then to use the same requirements for all future hardness assurance part procurement activity. Therefore, the hardness assurance design documentation (HADD) must include all the information needed to implement hardness assurance procedures.

5.3.1 HCC-1M parts. As previously indicated, parts which are categorized as HCC-1M require lot acceptance testing before use in the system. For dose-rate effects, the hardness assurance lot acceptance tests may take a number of forms. They may be 100 percent tests of the lot (screens), or they may be sample tests. The 100 percent screens may apply only to some upset and latchup tests, and will be discussed later. Alternately, some tests for upset and most burnout tests may be degrading because of the high current flows, and therefore must depend on sample tests.

5.3.1.1 Lot tolerance percent defective (LTPD). Two general methods may be used for lot acceptance tests. The first is called an attribute sampling test method or, more commonly, a lot tolerance percent defective (LTPD) test. This method specifies how many devices out of a given sample size can fail under a given test condition, and still meet an acceptance criterion (see appendix C). The LTPD method is widely used for quality assurance. It is simple to use, but requires inordinately large sample sizes when low failure probabilities with a high level of confidence are needed. For example, to allow prediction of a failure probability of 1 in 10- at 90 percent confidence, about 2,000 sample parts would have to be tested with no failures. Alternatively it may be possible to obtain high survival probabilities with a small sample size by performing an LTPD test at several times the specification dose rate; the extrapolation to higher survival probabilities at the specification fluence can be done using a knowledge of the probability distribution.

5.3.1.2 Variables sampling test method. The second method, called a variables sampling test method, determines the statistical behavior of a variable (e.g., dose-rate upset threshold) under test conditions. This method has the advantage of being able to predict a low failure probability, with high confidence, on the basis of a relatively small sample size. It has the disadvantage that it requires assumptions about the probability distribution of the variable involved. Such assumptions are usually reasonable, however, and the advantage of being able to use sample sizes which are easily attainable far outweighs any disadvantages.

5.3.2 Upset testing. Upset testing is identified as a nondestructive test method, and therefore can sometimes be imposed as a 100 percent screen on devices used in a system. However, a 100 percent screen is not always the solution to assuring hardness. Moreover, there is some controversy concerning the effects of dose-rate screening with the generation of latent defects due to the large current surges which result from this testing. Thus, while dose-rate screens may be used, a full characterization of the device type is recommended prior to 100 percent screening.

5.3.2.1 Test issues. There are several factors to consider when upset tests are performed. For example, if the device is a combinational logic device, the device may spontaneously recover from upset within some recovery time. One therefore may be concerned with either the upset level or the recovery time for the device, depending upon whether or not the circuit in which it is used is designed to be upset tolerant. Should the device be a sequential logic device, the state may be restored only through reinitialization after the radiation pulse. In this case, the upset level may be the parameter of importance. On the other hand, recovery time may be the parameter of interest, particularly for linear devices because they often saturate when exposed to the dose-rate environment.

5.3.2.2 Number of pulses. In all cases, the number of pulses required to determine the upset level contributes to the total dose exposure of the device. The total dose exposure may be particularly important for MSI or LSI devices where large numbers of state vectors may need to be tested. These cases may again force the use of sample tests.

5.3.2.3 Nondestructive tests - screens. The radiation characterization tests and the required circuit upset tolerance will determine the survivability level required for devices. For less complex devices, a 100 percent test of the devices at the required level maybe sufficient to qualify the part. The total dose accumulation and the overstress of the devices subjected to the 100 percent screen are factors which will need to be considered when deciding on screening tests for the devices.

5.3.2.4 Destructive tests - acceptance tests. In some cases, the devices may be damaged in determining either the upset threshold or the survivability level. In these cases the tests must be performed on samples and the appropriate procedures used for lot acceptance. An adequate sample size, consistent with a desired confidence and survival probability, must be chosen (see MIL-HDBK 816 and appendix B herein).

5.3.3 Burnout tests. Acquiring data to assess the burnout susceptibility of devices in the dose-rate environment presents a unique problem. Burnout characterization tests are only sometimes performed in the dose-rate environment. The burnout or damage levels whereby devices are compared are usually determined by pulse power testing of the device to failure. Therefore, burnout tests are always sample tests and statistical inference must be made.

5.3.3.1 Pulsed power tests. Most burnout tests are performed by applying an electrical overstress to the device, and measuring the stress to failure for a given pulse duration. There are obvious problems associated with this method of measurement. Some of these are: (a) the pulse duration; (b) failure statistics; and (c) correlation with dose-rate-induced burnout mechanisms.

5.3.3.1.1 Pulse power duration. The pulse power tests are usually performed at some pulse duration comparable to the expected duration of the dose-rate-induced photocurrent. The power to failure is usually assumed to follow the Wunsch-Bell power law, for time regimes between approximately 100 ns to a few microseconds,

$$POWER_F = K\ t^{-1/2},$$

which allows the extrapolation of the failure power (P_F) to times comparable to the photocurrent pulse duration.

5.3.3.1.2 Statistical analysis. Statistical analysis is usually performed using log-normal statistics on the stress to failure and acceptable design margins are applied. The choice of log-normal statistics is a convenient choice, providing a consistent approach. However, it is not certain that the log-normal statistics are the correct ones to use.

5.3.3.1.3 Log-normal statistics. The use of the log-normal statistics allows the application PCC method with its mathematical formalism. Another approach which is sometimes used is to determine the failure threshold for devices by data analysis and to apply a derating factor based on engineering judgement. In this way, a DMBP value may be chosen, and the DMBP method applied.

5.3.4 Latchup tests. Latchup can be a low probability failure mode, and therefore is impractical to approach using sample statistics. The usual hardness assurance test applied to latchup prone devices is a latchup screen. The screen is applied to 100 percent of the devices, and all devices which latch are rejected from use in the system.

5.3.4.1 Problems. There are significant problems with the use of a latchup screen. Possible uncertainties in the screening tests suggest that system-level solutions should be used if latchup-prone devices cannot be eliminated from the design. The uncertainties and cautions to be observed are discussed in 5.2.2.1.

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APPENDIX A

DOSE-RATE EFFECTS

10. SCOPE

10.1 Scope. This appendix covers the effects of photocurrents on semiconductor devices. This appendix is a mandatory part of the handbook. The information contained herein is intended for guidance only.

10.2 Device photoresponse. The principal dose-rate effect in semiconductor junctions is the generation of photocurrents. The photocurrents arise in devices when high-energy particles such as gamma rays, x-rays or electrons are absorbed and create excess electron-hole pairs in the material of the device. The collection of these excess carriers by the device junction results in current flow in the device.

10.2.1 Device photoresponse. The theory of junction photocurrents is well understood, and can be calculated for most normal ionization sources and simple device geometries. For an incident dose-rate pulse, the transient photocurrent collected by a PN junction is approximately:

$$I_p = q\,g\,A\,\dot{\gamma}\,W\left[L_p \operatorname{erf}\left(\frac{t}{\tau_p}\right)^{1/2} + L_n \operatorname{erf}\left(\frac{t}{\tau_n}\right)^{1/2}\right] ,$$

where

q is the electron change
A is the junction area,
W is the width of the junction depletion region,
Ln is the minority carrier diffusion length of electrons in p material,
L_p is the minority carrier diffusion length of holes in n material,
p is the corresponding minority carrier lifetime, and
g is the carrier generation rate.

$g = 4.2 \times 10^{13}$ hole-electron pairs/cm3-rad(Si)

where $\dot{\gamma}$ is the radiation dose-rate in rads(Si)/s. A similar decay occurs at the termination of the radiation pulse.

10.2.2 Long pulse. For a radiation pulse which is long with respect to the minority carrier lifetime, the photocurrent reaches a steady-state value of:

$$I_p = q\,Ag\,(W + L_p + L_n)\,\dot{\gamma} = q\,Ag\,L_{eff}\,\dot{\gamma}$$

where L_{eff} is the effective minority carrier collection length around the PN junction. L_{eff} is the sum of the depletion layer width and the diffusion lengths on each side of the junction.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. DOSE-RATE FAILURE

30.1 Dose-rate failure. The photocurrent dose-rate transient failure threshold for an integrated circuit is normally defined as the radiation level required to produce an output voltage which is sufficiently large to cause a change of state in subsequent logic stages or a change of state of stored data or logic state.

40. CORRECTIVE ACTION

40.1 Unwanted photocurrents. The photocurrent generation in devices acts as an internal current generator in parallel with each of the PN junctions in the device. The approach to hardening devices to dose-rate effects is to eliminate, reduce, or to compensate for the unwanted photocurrents. Some of the major techniques which are used are:

a. Minimize the number of reversed biased junctions in order to reduce the photocurrent.

b. Increase the operating current density in the device by decreasing the junction area, or by increasing the operating current.

c. Minimize the collection depth in order to reduce the collection volume.

d. Compensate for the photocurrents which flow by adding semiconductor elements to the circuit.

40.2 Minimizing junctions. This technique can be achieved by the use of such techniques as dielectric isolation and thin-film resistors in device construction. The goal is to have no more than two junctions in any conduction area.

40.3 Increasing current density. This technique reduces the relative amount of photocurrent with respect to the device operating current. Since the photocurrent is area dependent, one method of increasing the current density is to reduce the device junction size.

40.4 Minimizing collection depth. This method can be implemented by reducing the lifetime in the collection region of the device by use of some lifetime killing method such as gold doping. The collection volume can also be reduced by the use of very thin layers on insulating substrates, such as in SOS or SOI technology.

40.5 Compensation. This technique places semiconductor junctions across the base emitter junction of devices in order to shunt the generated photocurrents away from the device base region. In this way, the photocurrent does not cause unwanted voltage drops in the devices, and does not undergo amplification by the active devices in the circuits.

50. TRANSIENT UPSET HARDNESS

50.1 Transient upset thresholds. Typical transient upset thresholds for several technologies are shown on figure 4. It should be noted that there may be considerable variation in the upset threshold for various members of a family of devices within a technology type. This is because of the strong dependance of upset on the quality of the power bussing and on the layout. Any one family within a technology may cover the entire range shown.

50.2 Observations. Some general observations can be made. TTL devices seem to have comparable upset thresholds regardless of the level of integration. NMOS is the most sensitive technology for transient upset, while CMOS seems to be the second most sensitive technology. CMOS/SOS, on the other hand, exhibits a high threshold level for upset because of the reduced collection volume for photocurrents.

50.3 Latchup thresholds. Typical latchup thresholds for these families of devices are shown on figure 5. Latchup is a phenomenon which is very much device dependent as well as technology dependent. The incidence of latchup in bulk CMOS is high, while the incidence in some families of TTL devices is extremely low.

60. REFERENCES

60.1 References. The documents listed in this section where used as references for the preparation of this document.

60.1.1 F. L. Wirth and S. C. Rogers, "The Transient Response of Transistors and Diodes to Ionizing Radiation," IEEE Trans. on Nucl. Sci., NS- 11, No. 5, November 1964.

60.1.2 J. F. Leavy and R. A. Poll, "Radiation-Induced Integrated Circuit Latchup," IEEE Trans. on Nucl. Sci., NS-16, No. 6, December 1969.

60.1.3 M. Simons, et al., "Integrated Circuits for Radiation-Hardened Systems: A State-of-the-Art Review," AFAL Report AFAL-TR-76-194, January 1977.

60.1.4 D. M. Long, "State-of-the-Art Review: Hardness of MOS and Bipolar Integrated Circuits," IEEE Trans. on Nucl. Sci., NS-27, No. 6, December 1980.

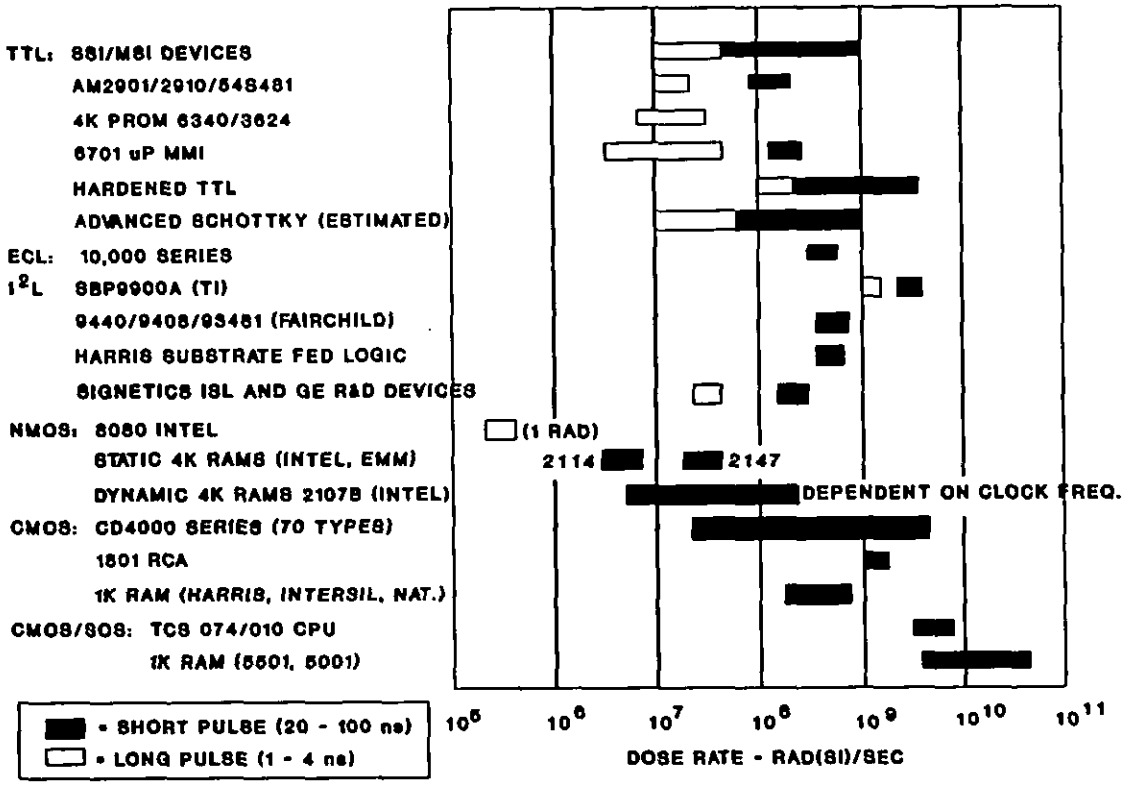

FIGURE 4. Transient upset hardness.

TTL: 6701 uP MMI (1976)
6S8100 FPLA MMI (1976)
82S11 1K RAM SIGNETICS (1979)
EARLY 54LS193
HUNDREDS OF THOUSANDS OF SSI/MSI UNITS TESTED WITHOUT LATCHUP.

HARDENED TTL: LATCHUP PREVENTED BY DIELECTRIC ISOLATION.

ECL: LATCHUP NOT OBSERVED (LIMITED TEST DATA)

I^2L: LATCHUP PREVENTED BY LOW SUPPLY VOLTAGE.

NMOS: NO PNPN PATHS FOR LATCHUP.

CMOS: • CD4000 SERIES (70 TYPES, 40 LATCHED) 10V
NEITRON IRRADIATED CD4000 (NO LATCHUP 70 TYPES, 10V)
CDP 1802 uP (RCA)
6508 1K RAM (HARRIS, INTERSIL) 5V

CMOS/SOS: LATCHUP PREVENTED BY SAPPHIRE ISOLATION.

LINEAR ICs: SOME PART EXHIBIT LATCHUP.

• USE OF GOLD DOPING OR EPI STRUCTURE ALSO HAS POTENTIAL TO PREVENT LATCHUP.

■ • RANGE OF OBSERVED LATCHES
□ • OBSERVED LATCHUP THRESHOLD

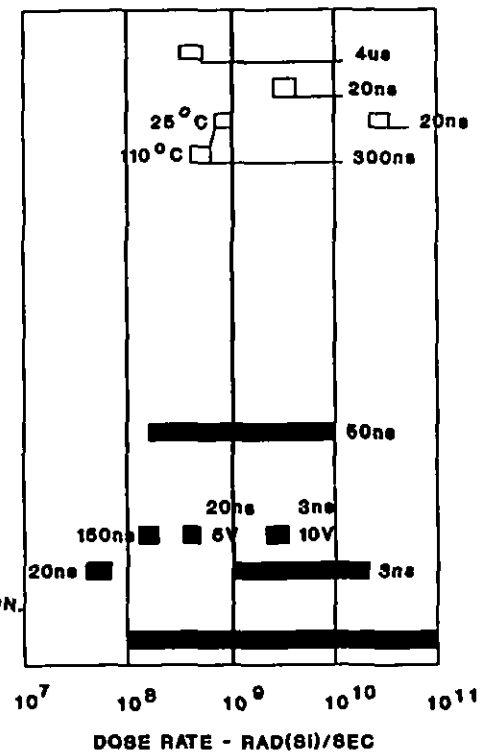

FIGURE 5. Latchup thresholds.

APPENDIX B

DOSE-RATE TESTING

10. SCOPE

10.1 Scope. This appendix covers the various radiation sources used when performing dose-rate testing. This appendix is a mandatory part of the handbook. The information contained herein is intended for guidance only.

10.2 Radiation testing. The most common radiation sources which are used for dose-rate testing of semiconductor components are the linear accelerator (Linac) and the flash x-ray (FXR) machine. Because of the wide variety of components, and much wider variety of ways that a component may be used in a circuit, a radiation test plan and report are required for the proper documentation and performance of the tests. Except for dosimetry, test details will vary from one device type to another.

10.2.1 Linacs. In general Linacs are useful for testing devices in dose-rate ranges from 1×10^6 to 1×10^{11} rads(Si)/s, with variable pulsewidths.

10.2.2 FXRs. FXR machines cover the same dose-rate range. A few large machines can reach 10^{12}rads(Si)/s. Those that can be operated in the electron beam mode can go above 10^{13}rads(Si)/s. All operate at only at a single pulsewidth.

20. APPLICABLE DOCUMENTS

20.1 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM E 666	Standard Method for Calculation of Absorbed Dose from Gamma or X Radiation.
ASTM E 668	Practice for the Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.
ASTM E 820	Standard Practice for Determining Absolute Absorbed Dose Rates for Electron Beams.
ASTM F 448	Standard Method for Measuring Steady-State Primary Photocurrent.
ASTM F 526	Method of Dose Measurement for Use in Linear Accelerator Pulsed Radiation Effects Tests.

(Copies of these documents may be obtained from American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103-1187.)

Note: Several standard test methods and standard practices have been developed for use in measuring the ionizing radiation environment. These documents should be consulted when radiation tests are performed.

A number of relevant test methods are available in the military standards system. The following can be found in MIL-STD-883:

Method 1020	"Radiation-Induced Latchup Test Procedure,".
Method 1021	"Dose Rate Threshold for Upset of Digital Microcircuits,".
Method 1023	"Dose Rate Response of Linear Microcircuits,".

30. CAUTIONS

30.1 Cautions. There are a number of test variables which must be considered when dose-rate tests are performed. Clearly, good engineering practice must be exercised, and correct radiation test procedures must be followed. Some of the test concerns are as follows.

30.1.1 Air ionization. The radiation pulse can cause air ionization which can result in a spurious component of the measured signal. The presence of these signals can be checked by irradiation of the test fixture without the device being installed. The effect can be minimized by coating the DUT chip and bond wires with silicone or a similar material.

30.1.2 Secondary emission. Charge emission from, or charge injection into, the test device and test circuit can also result in a spurious component of the measured signal. In contrast to air ionization, secondary emission effects are generally not field dependent, and therefore it is possible to separate the two effects. Secondary emission can be reduced by shielding the surrounding area and irradiating the device only.

30.1.3 Orientation. The effective dose to the semiconductor device can be altered by orientation. Severe dose gradients in a radiation field, along with package shielding may result in nonuniform, and even unknown doses in regions of the devices. Care must be taken in the positioning of devices in the radiation field.

30.1.4 Dose enhancement. High atomic number material near the active regions of the test device can cause an enhancement of the dose delivered to sensitive regions of the device when the device is irradiated at an FXR. The effect is energy dependent, increasing with lower energies. The extent of this effect must be considered in any FXR dose-rate testing.

30.1.5 Noise. Most pulsed radiation facilities are inherent sources of r-f noise. Such noise minimizing techniques as single-point ground, filtered power supply lines, etc., must be used when attempts are made to make quality data measurements through the radiation pulse.

30.1.6 Dosimetry. Accurate dose-rate monitors for dose-rate testing are not readily available. Generally, the total dose delivered in each pulse is measured along with some type of measurement of the pulse shape. The dose rate is then calculated. Good dosimetry practice must be used in order to provide accurate dose-rate values.

30.1.7 Temperature. Many dose-rate effects are temperature sensitive. A notable example is latchup in integrated circuits. The temperature during the test should be controlled, and for latchup, aa elevated test temperature must be chosen.

30.1.8 Total dose. Some dose-rate effects, such as upset, are generally nondestructive to the device. Therefore, some devices may be screened on a 100 percent basis to determine the upset threshold. However, each pulse of the radiation source imparts some total dose to the device. The accumulated total dose delivered to the device during dose-rate testing may alter the response of the device or cause total dose failure. Care must be taken to ensure that the total dose delivered to the device during dose-rate testing does not cause damage to the device which can mask the dose rate effects.

40. REFERENCES

40.1 References. The documents listed in this section where used as references for the preparation of this appendix.

40.1.1 "TREE Preferred Procedures, Selected Electronic Parts," DNA 2028H, January 31, 1982.

40.1.2 "Practice for the Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices," ASTM E 668.

40.1.3 "Method of Dose Measurement for Use in Linear Accelerator Pulsed Radiation Effects Tests," ASTM E 526.

APPENDIX C

ONE-SIDED TOLERANCE FACTORS

10. SCOPE

10.1 Scope. The purpose of this appendix is to present some of the techniques necessary for dose-rate hardness assurance. A complete treatment is not given, only the information required to use this document is presented. This appendix is a mandatory part of the handbook. The information contained herein is intended for guidance only.

10.1.1 Overview. Hardness assurance applications generally involve statistical techniques to determine the adequacy of design margins in achieving required survival probabilities. The statistical question is addressed well in appendix E of DNA 5910F, "Piece Part Neutron Hardness Assurance Guidelines for Semiconductor Devices", and should be consulted for questions involving statistics.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. SAMPLING

30.1 Sampling. Most hardness assurance techniques require some sort of sampling and statistical extrapolation to the parent population. The results of sampling are most frequently reported in terms of a confidence, C, that at least a proportion, P, of the lot will not fail under actual test.

30.1.1 Tests. Two kinds of test are often performed on the selected sample to determine the population characteristics.

30.1.1.1 Sampling by attribute. The first is termed "sampling by attribute." In sampling by attribute, some characteristic of the item is monitored. For example, upset testing at a single dose rate would determine whether or not the semiconductor devices within a selected sample of devices would upset or not at that dose rate. This would be a "go-no-go" situation. Either the device upset or not at the particular dose rate. No information would be obtained on the exact threshold for upset or the distribution of the threshold for upset. This kind of test is often handled by using the method of Lot Tolerance Percent Defective (LTPD), to make predictions about failure probabilities.

30.1.1.2 Sampling by variable. The second method of sampling is termed "sampling by variable." In this case, a measurement is made of some critical parameter in a sample. For example, the upset threshold of each semiconductor device in a sample may be measured in terms of the threshold dose rate for upset. Sampling by variable lends itself well to the application of statistical techniques, provided the statistical distribution of the data is known.

30.2 Normal and log-normal statistics. For hardness assurance applications, normal and log-normal statistics are often used (see 50.1.1 herein). A check should always be made to see if the application of a particular statistical distribution to the data is proper. Most often, for radiation effects, the log-normal distribution is assumed, even though the actual distribution of data is not known. There is evidence that even if the log-normal distribution is not exactly correct, its use can still provide good engineering approximations to the hardness assurance problem. In log-normal distribution, the logarithms of the quantities are distributed normally.

40. SAMPLING BY VARIABLES - ONE-SIDED TOLERANCE LIMITS

40.1 One-sided tolerance limits. One statistical technique used with sampling by variable data is the method known as the one-sided tolerance limit. If a parameter is known to be normally distributed, then the estimates of lot quality can be obtained with small samples. Thus, if the parameter, x, is normally distributed (x may be the logarithm of a parameter), and n items are sampled, then a lot is rejected if the limiting quantity, L, exceeds a value, LMAX, where

$$L = m + K_{TL}(n,C,P)s,$$

where

m is the measured mean of the sample,

s is the standard deviation of the sample,

C is the required confidence level, and

P is the required survival probability, or lot quality.

The one-sided tolerance limit factor, K_{TL}, is a function of the sample size, n, the confidence, C, and the lot quality, P. The statistical statement that can be made is that if more than the proportion, P, devices of the parent distribution has values of x less than L_{MAX}, then the lot will be rejected with probability, C. L_{MAX} may be a parameter selected such that if its value is exceeded, then failure will occur.

40.2 Minimum parameter formulation. In many hardness assurance applications, the critical parameter may be a minimum and not a maximum. The formulation is similar, and a lot is rejected if the quantity, L, is less than L_{MIN} where

$$L = m - K_{TL}\ (n,C,P)s,$$

where the quantities have been previously defined. In this case, LMIN may be a parameter value, selected such that if the actual value falls below this value, system-failure will occur.

40.3 One-sided tolerance. Table VIII is a table of one-sided tolerance factors for some of the most frequently used lot qualities and 90 percent confidence.

TABLE VIII. One-sided tolerance limits, K_{TL}.

	C = 0.9				
			P		
N	0.9	0.95	0.99	0.999	0.9999
3	4.259	5.311	7.340	9.651	11.566
4	3.188	3.957	5.438	7.129	8.533
5	2.742	3.400	4.666	6.111	7.311
6	2.493	3.091	4.243	5.555	6.645
7	2.332	2.894	3.972	5.202	6.222
8	2.218	2.755	3.783	4.955	5.927
9	2.133	2.649	3.641	4.771	5.708
1	2.065	2.568	3.532	4.628	5.538
1	2.011	2.503	3.443	4.514	5.402
1	1.966	2.448	3.371	4.420	5.290
1	1.928	2.403	3.309	4.341	5.196
1	1.895	2.363	3.257	4.273	5.116
1	1.867	2.329	3.212	4.215	5.046
1	1.842	2.299	3.172	4.164	4.986
1	1.819	2.272	3.137	4.119	4.932
1	1.800	2.249	3.105	4.078	4.884
1	1.781	2.228	3.077	4.042	4.841
2	1.765	2.208	3.052	4.089	4.802
2	1.750	2.190	3.028	3.979	4.766
2	1.736	2.174	3.006	3.952	4.734
2	1.724	2.159	2.987	3.926	4.704
2	1.712	2.145	2.969	3.903	4.677
2	1.701	2.132	2.952	3.882	4.651
3	1.657	2.080	2.884	3.794	4.546
3	1.623	2.041	2.833	3.729	4.470
4	1.598	2.010	2.793	3.678	4.411
4	1.575	1.986	2.761	3.638	4.363
5	1.559	1.965	2.735	3.605	4.324
6	1.532	1.933	2.694	3.552	4.262
7	1.511	1.909	2.662	3.513	4.215
8	1.494	1.890	2.637	3.482	4.178
9	1.481	1.874	2.617	3.456	4.148
10	1.470	1.861	2.601	3.435	4.124

APPENDIX C

Factors K_{TL} such that with confidence, C, at least a proportion, P, of a normal distribution will be less than

$$\bar{x} + K_{TL}s.$$

50. REFERENCES

50.1 References. The documents listed in this section where used as references for the preparation of this document.

50.1.1 A. Namen on, et al., "Piece Part Neutron Hardness Assurance Guidelines for Semiconductor Devices," DNA 5910P, October 6, 1981.

50.1.2 "Military Specification, Microcircuits, General Specification For," MIL-M-38510, Appendix 13, Defense Logistics Agency, 1984.

50.1.3 "Military Standard Test Methods and Procedures for Microelectronics," MIL-STD-883C, August 1983.

CONCLUDING MATERIAL

Custodians:
Army - ER
Air Force - 19
DNA - OS
NASA - NA

Review activities:
Army - AR, MI, PA
Navy - MC
Air Force - 11, 17, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, OS, SH

Civil agency coordinating activities:
DOT-FAA-(RD-650)

Preparing activity:
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